

Compal Confidential

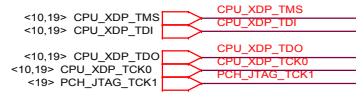
C5PRH MB Schematic Document

LA-E921P

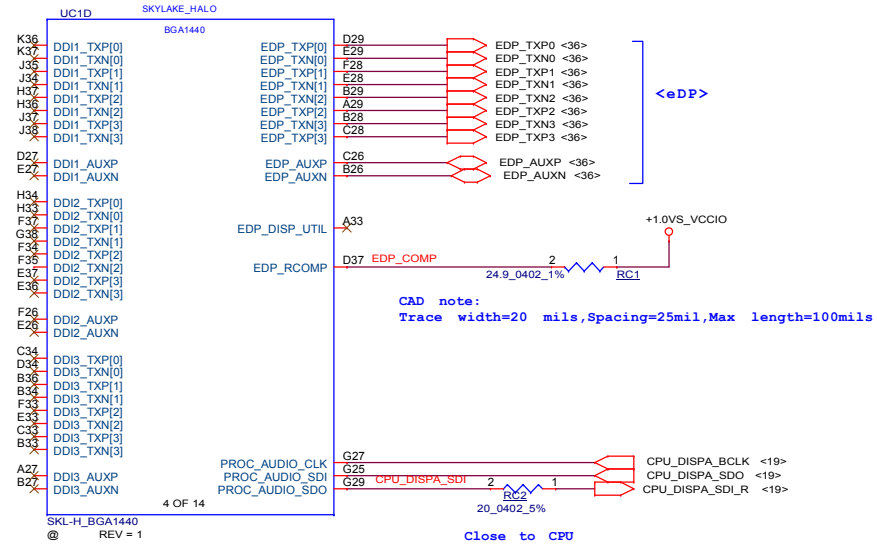
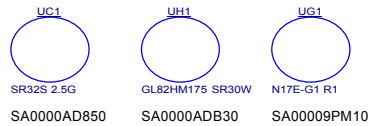
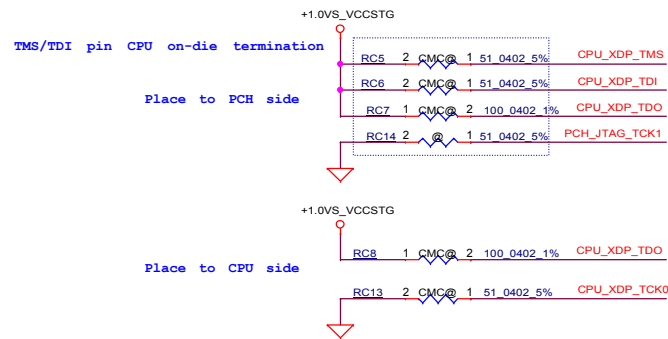
Rev:1.A

2017.03.29

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Issued Date	2016/12/15	Deciphered Date	2017/12/15	Title		
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				Size	Document Number	Rev
				Custom	C5PRH M/B LA-E921P	1.A
				Date:	Friday, March 31, 2017	Sheet 1 of 73

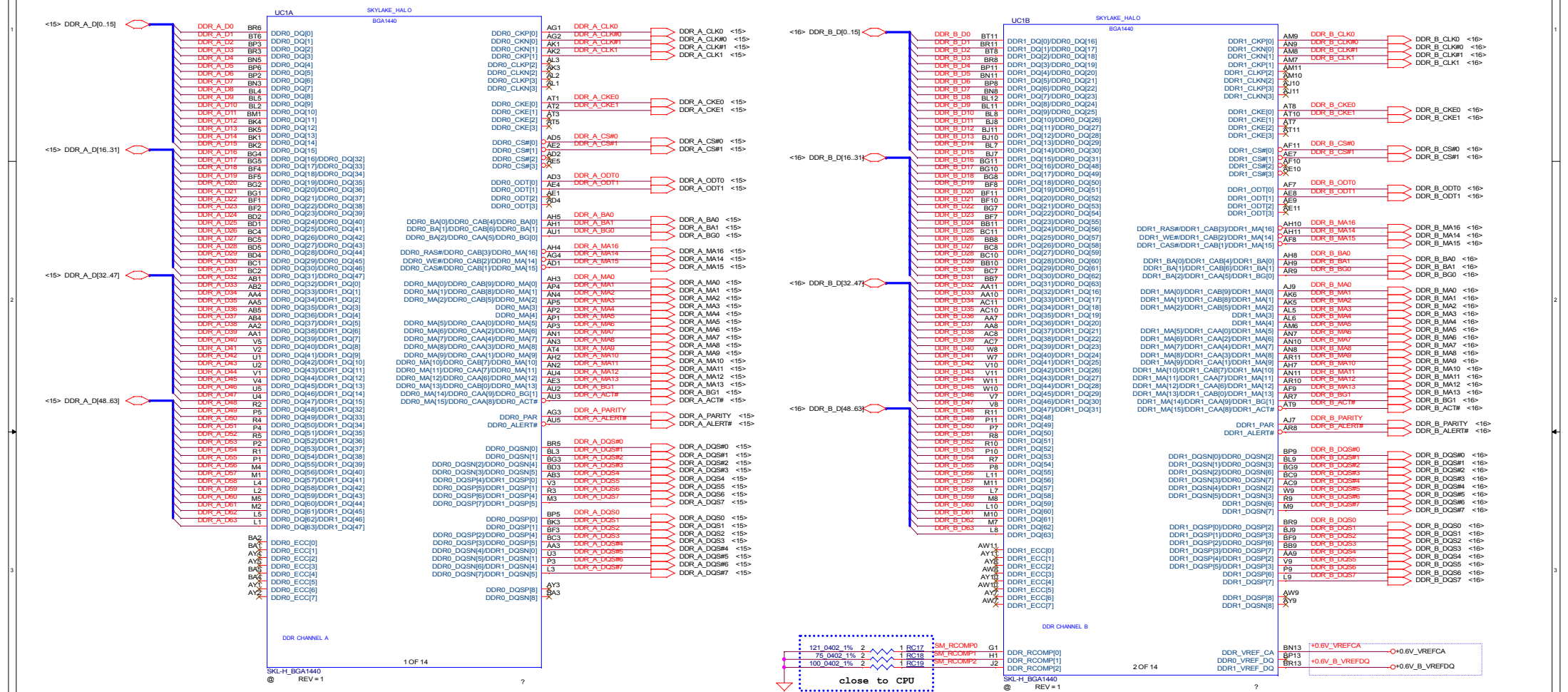


If need debug from usb port. this cmc@ need pop

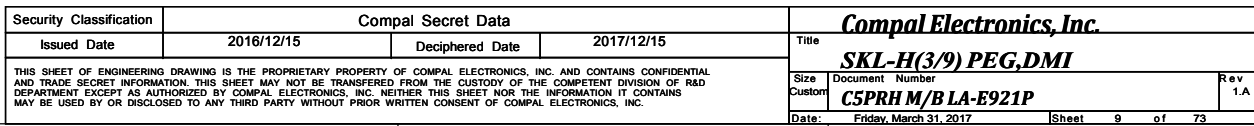


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Issued Date	2016/12/15	Deciphered Date	2017/12/15	SKL-H(1/9)DDI,EDP	
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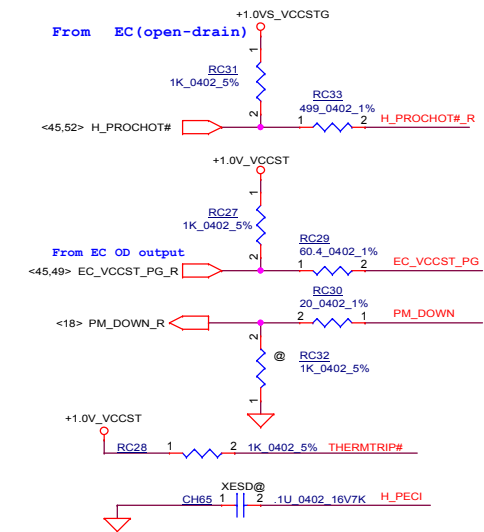
Interleaved Memory



Security Classification		Compal Secret Data		Title	
Issued Date	2016/12/15	Deciphered Date	2017/12/15	SKL-H(2/9)DDRIII	
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Place the PU resistors close to CPU

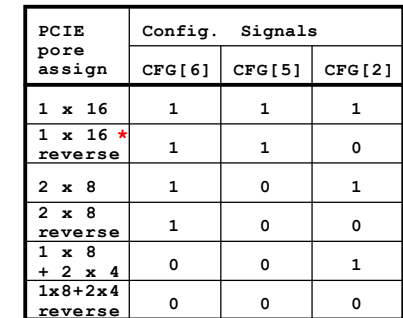
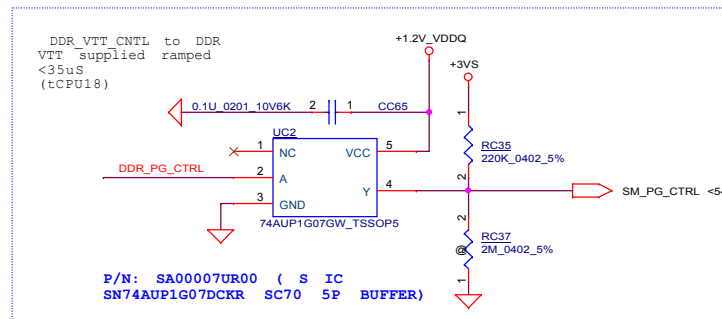


UC1E SKYLake_HALO

5 OF 14

SKL_H_BGA1440
REV = 1

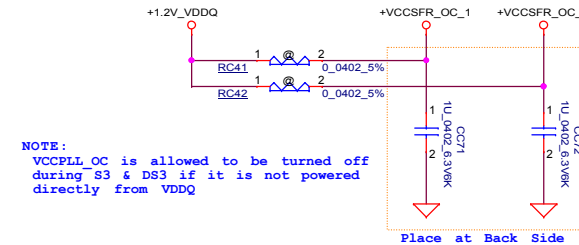
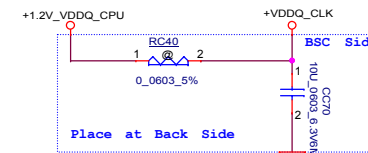
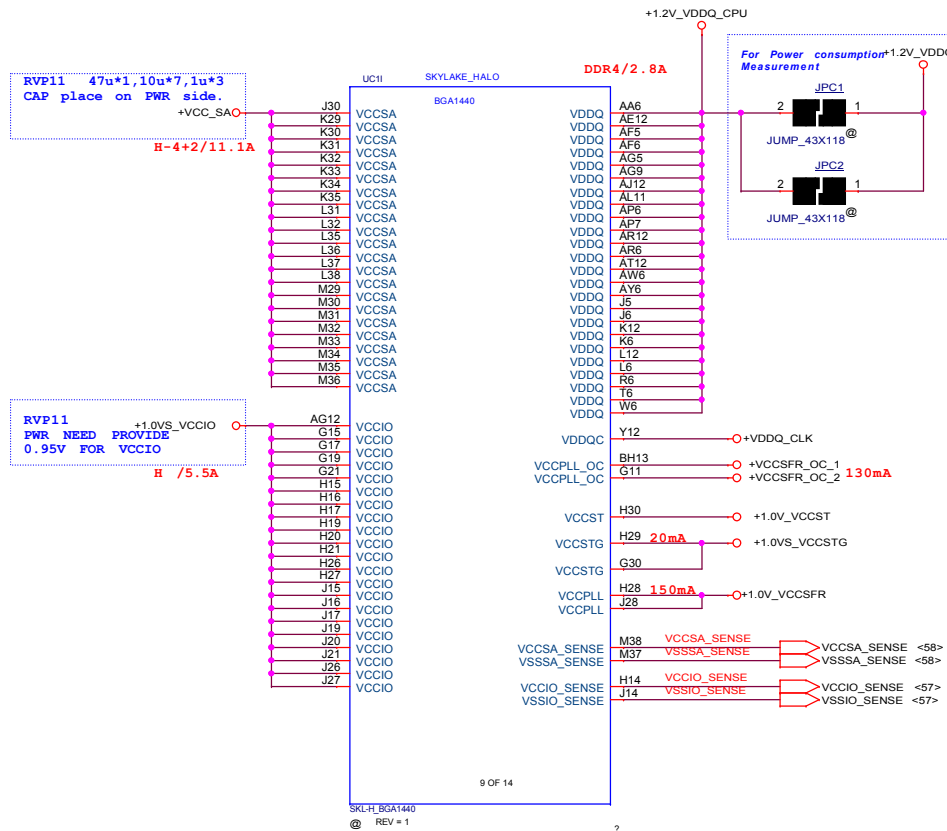
49.9_0402_1%



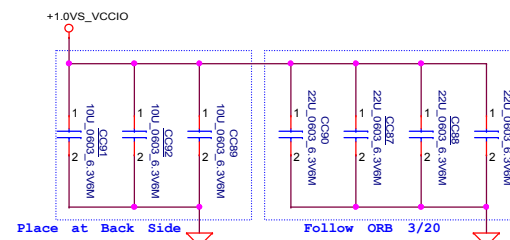
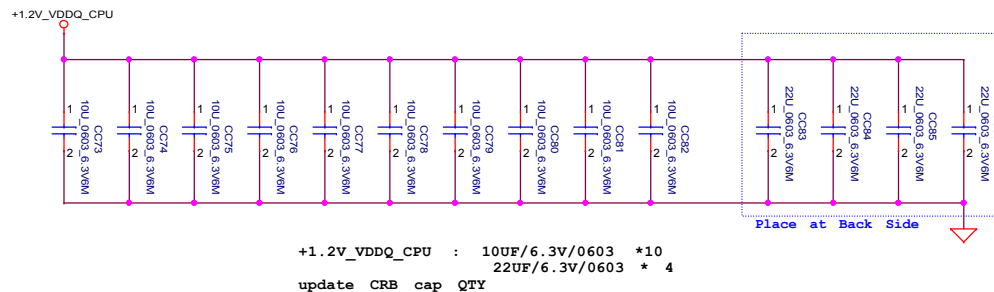
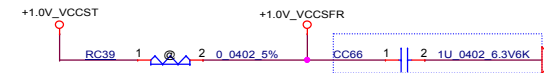
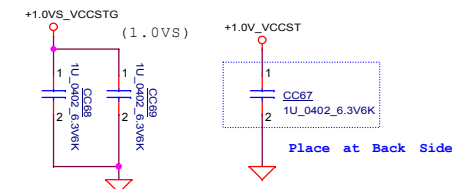
CFG signals internal PH default value = 1

	Description
CFG[0] *	Stall reset sequence after PCU PLL lock until de-asserted - 1 = (Default) Normal Operation; - No stall. - 0 = Stall.
CFG[4] *	Enable eDP - 1 = Disabled. - 0 = Enabled.
CFG[7] *	PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]	Reserved configuration lane.

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				CSPRH M/B LA-E921P	
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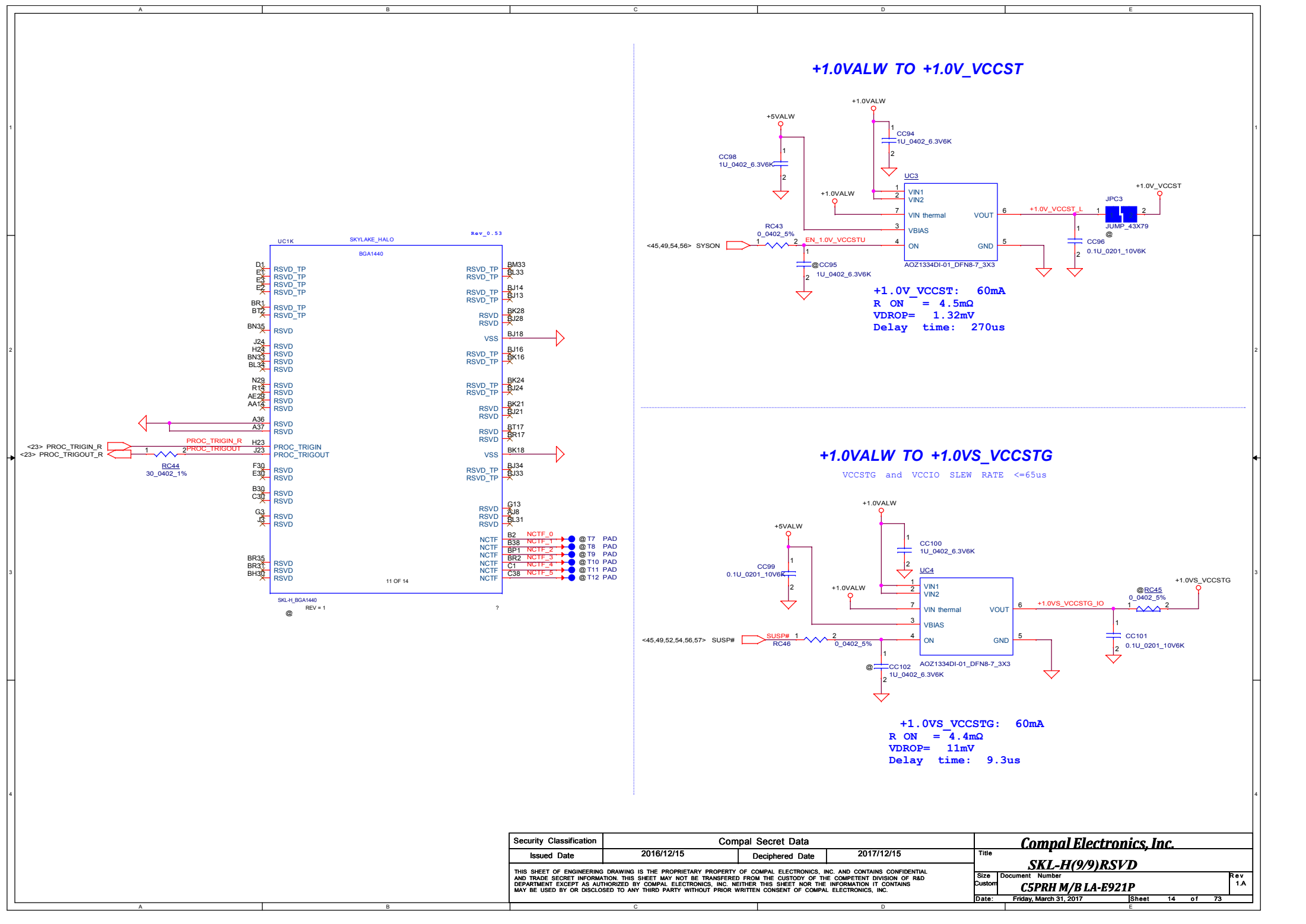


NOTE:
VCCPLL_OC is allowed to be turned off during S3 & DS3 if it is not powered directly from VDDQ

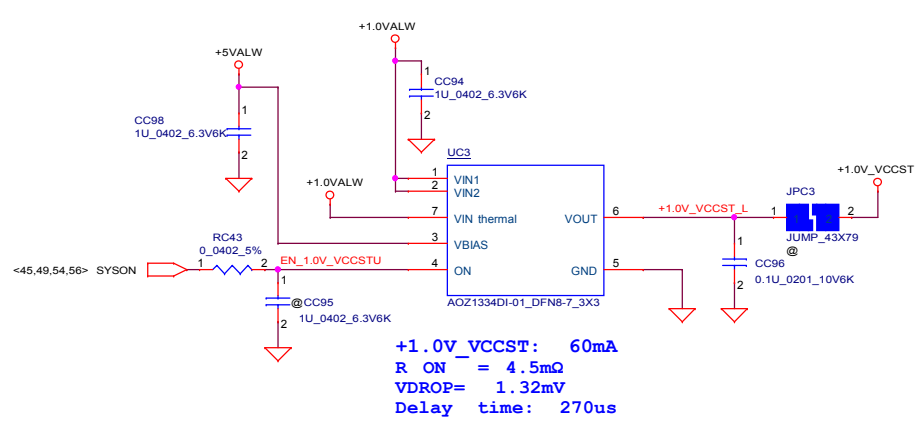


CPU_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

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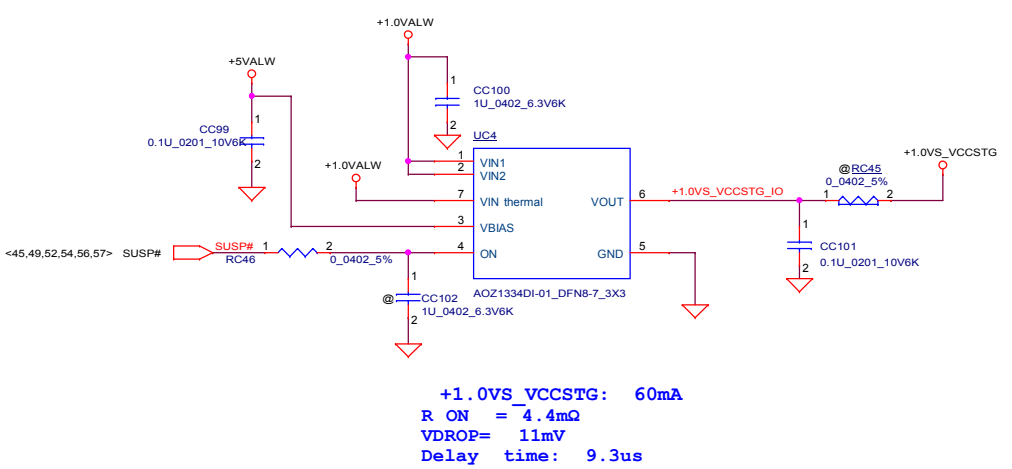


+1.0VALW TO +1.0V_VCCST



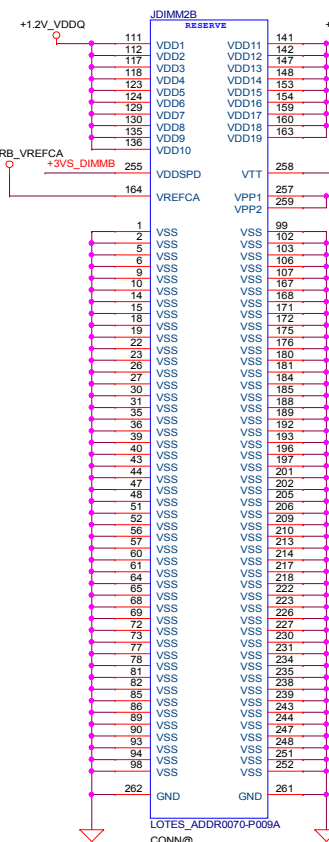
+1.0VALW TO +1.0VS_VCCSTG

VCCSTG and VCCIO SLEW RATE <=65us



Reverse Type-8H

2-3A to 1 DIMMs/channel

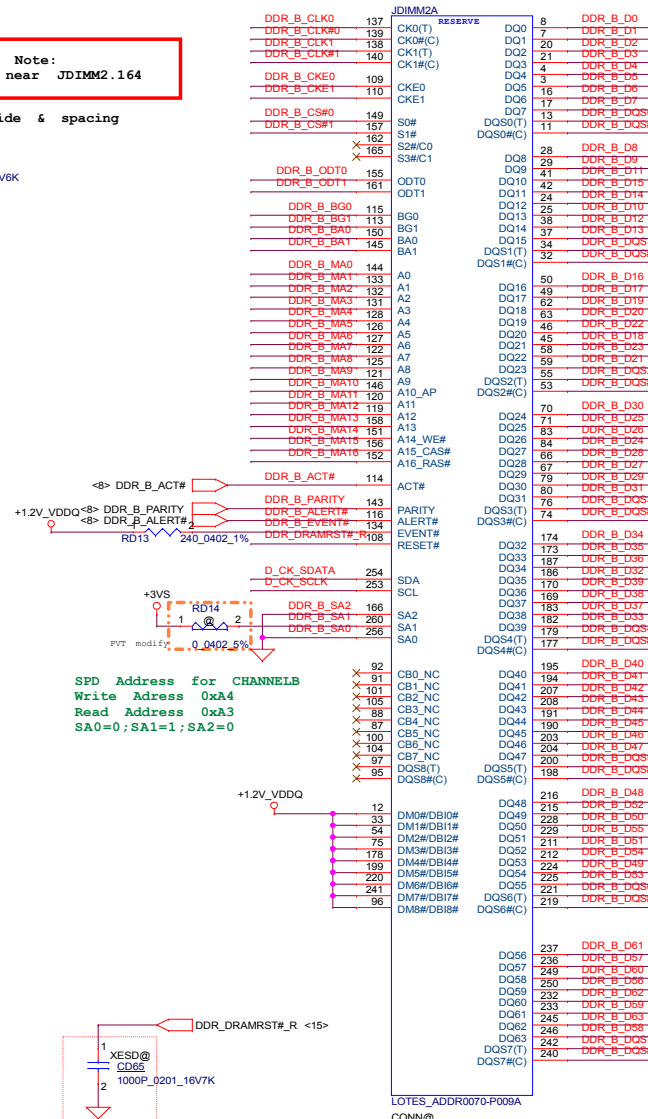


Interleaved Memory

Security Classification		Compal Secret Data		Title DDR4 DIMMB Size: Custom Document Number: CSPRH M/B LA-E921P Date: Friday March 31 2017 Sheet: 16 of 73
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Layout NOTE
PLACE THE CAP within 200mil from Pin108
*2015M0W02, Can't install Cap on DRAMRST

SPD Address for CHANNELB
Write Address 0xA4
Read Address 0xA3
SA0=0; SA1=1; SA2=0



Layout Note:
Place near JDIMM1.164
within 200mils

Layout Note:
Place near JDIMM2.257/259

Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM2.164

20mils wide & spacing

CD41
0.1U_0201_10V6K

CD39
0.1U_0201_10V6K

CD40
0.22U_0402_16V7K

CD41
0.1U_0201_10V6K

CD42
0.1U_0201_10V6K

CD43
0.1U_0201_10V6K

CD44
0.1U_0201_10V6K

CD45
0.1U_0201_10V6K

CD46
0.1U_0201_10V6K

CD47
0.1U_0201_10V6K

CD48
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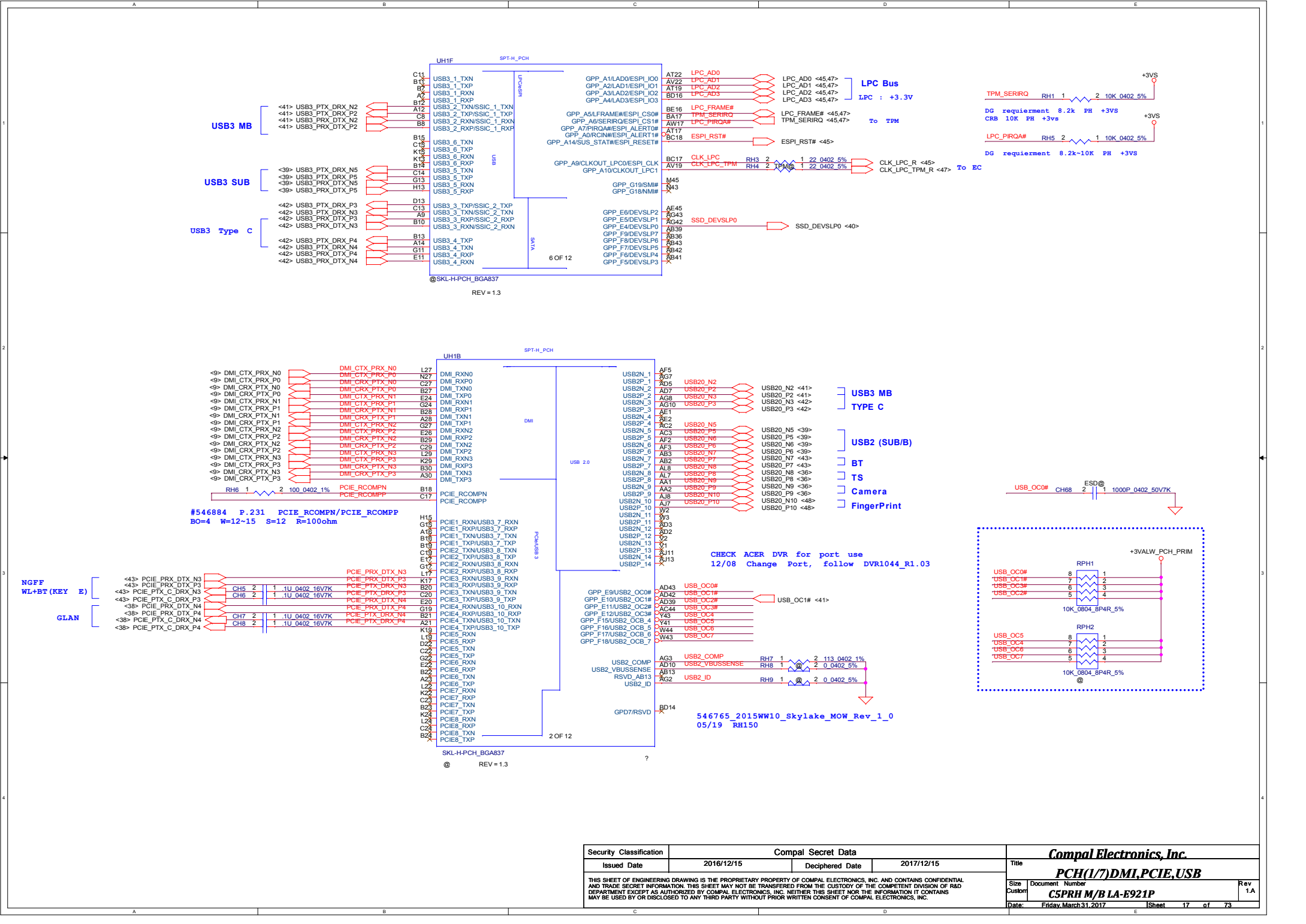
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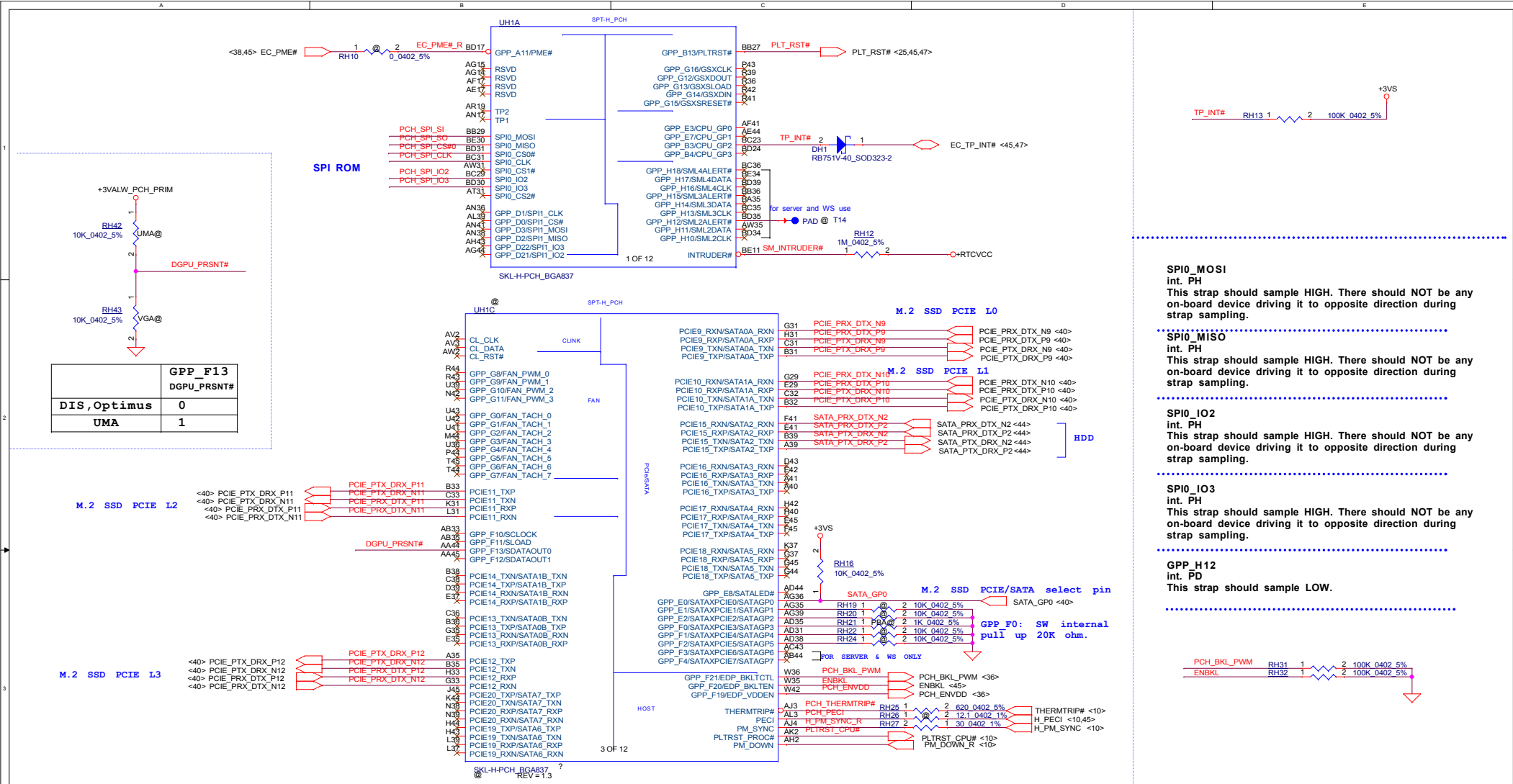
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CD230
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CD231
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						Size	Document Number	Rev
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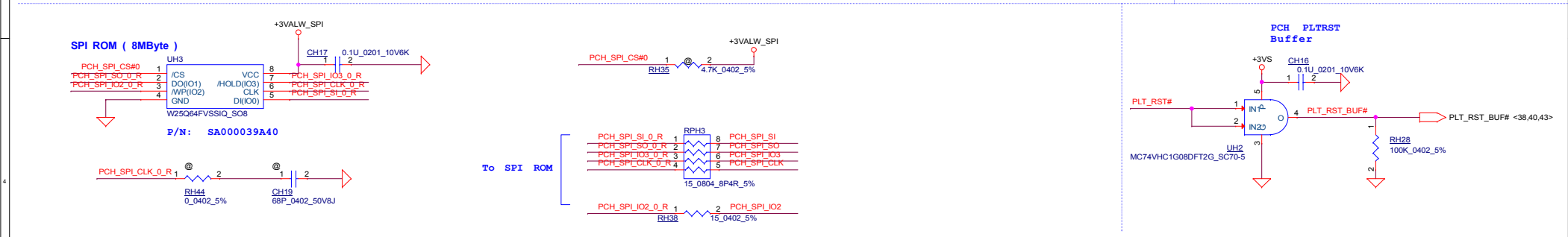
SPI0_MOSI
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MISO
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

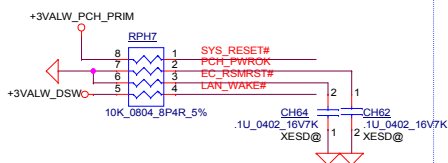
SPI0_IO2
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

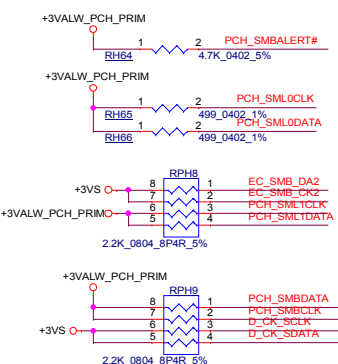
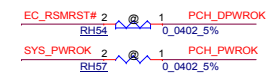
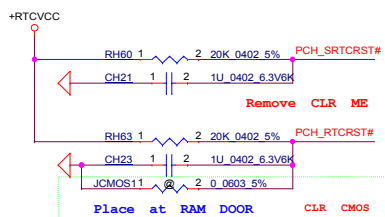
GPP_H12
int. PD
This strap should sample LOW.



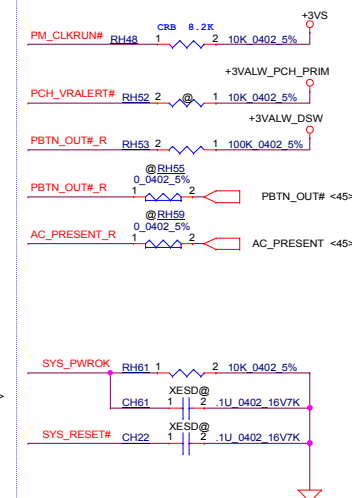
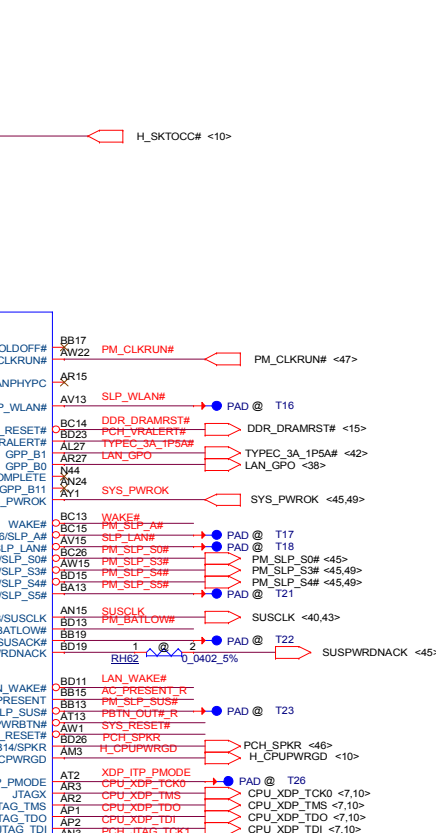
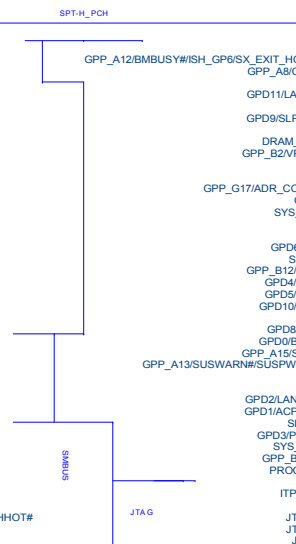
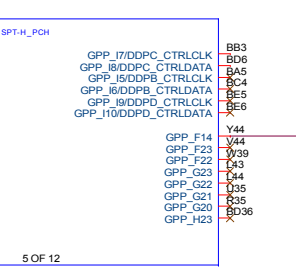
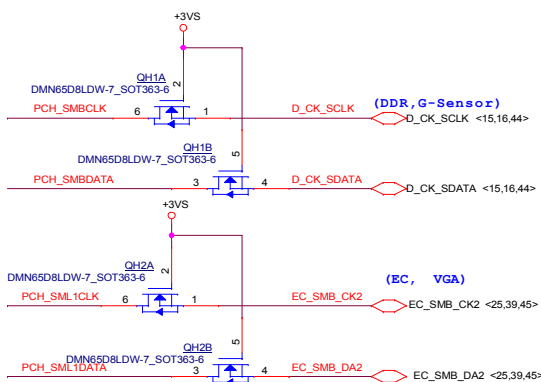
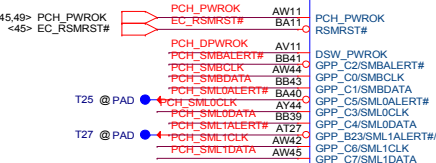
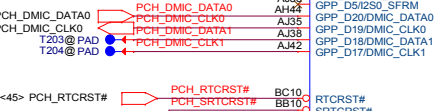
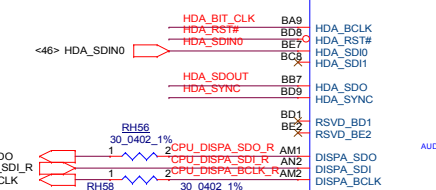
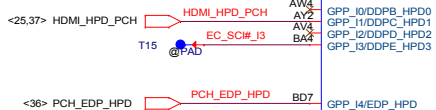
The diagram shows the timing for the RPH6 component. The input signal <45> ME_EN is connected to pin 1 of RPH6. The output signal HDA_SDOUT is connected to pin 8 of RPH6. The output signal HDA_RST# is connected to pin 7 of RPH6. The output signal HDA_SYNC is connected to pin 6 of RPH6. The output signal HDA_BIT_CLK is connected to pin 5 of RPH6. The timing parameters for the output signals are: HDA_SDOUT (0.0402_5%), HDA_RST# (0.0402_5%), HDA_SYNC (0.0402_5%), and HDA_BIT_CLK (0.0402_5%). The component is labeled RPH6 and has a timing parameter of 33 0804 8P4R 5%.



WAKE#
(DSX wake event)
10 K Ω pull-up to VccDS W3_3
The pull-up is required even if PCIe* interface
is not used on the platform.



PDG_0_71 requirement PH to +3V_PCH
10/14 Dan



SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable " Top Swap" mode. (Default)
1 = Enable " Top Swap" mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

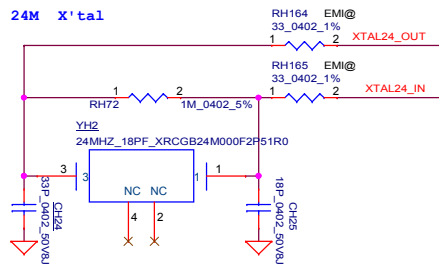
DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

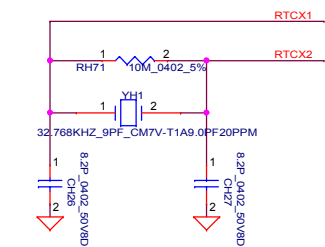
DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

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				Date: Friday, March 31, 2017	Sheet 19 of 73

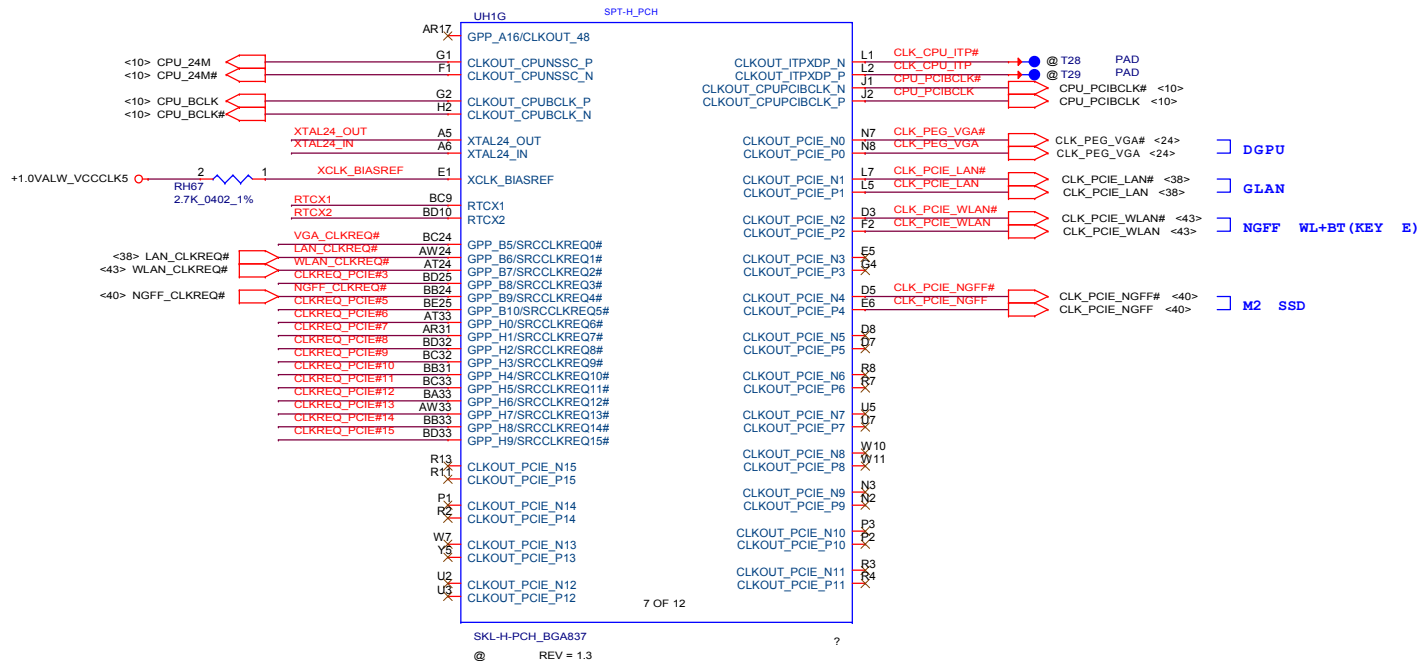
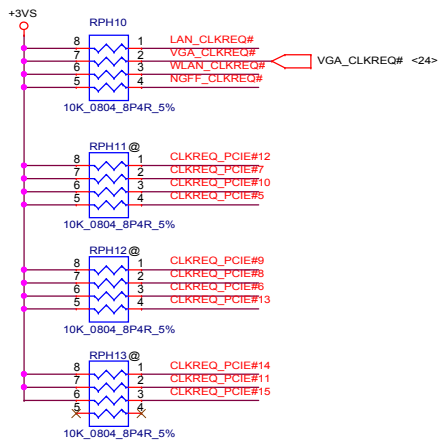
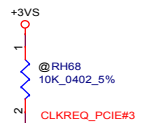
24M X'tal



RTC X'tal



P/N: SJ10000Q400 (S CRYSTAL 32.768KHZ 9PF 20PPM 9H03280012)



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Functional Strap Definitions

GSPI1_MOSI / GPP_B22

int. PD

Boot BIOS Destination

0 = SPI (Default)

1 = LPC

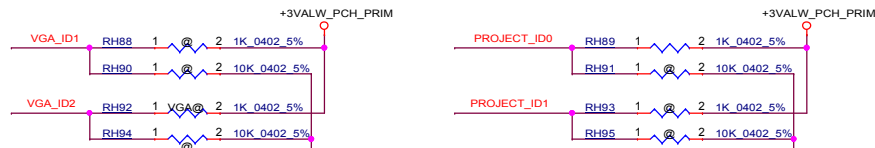
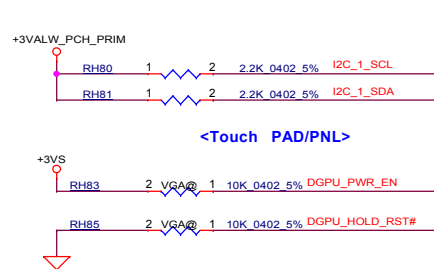
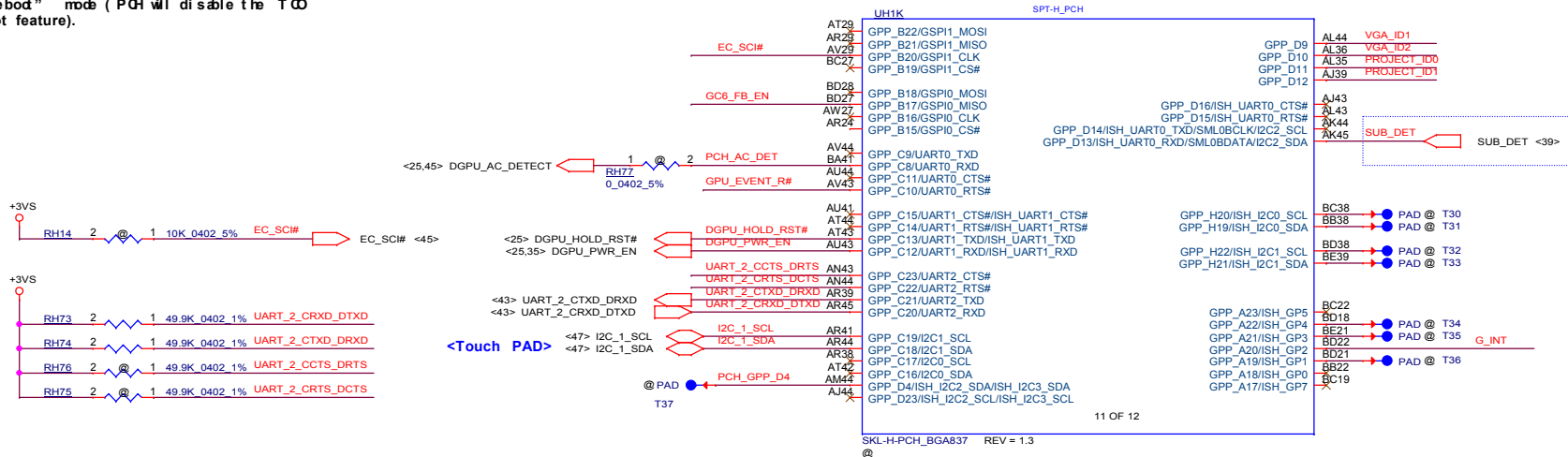
GSPI0_MOSI / GPP_B18

int. PD

0 = Disable " No Reboot" mode (Default)

1 = Enable " No Reboot" mode (PCH will disable the T

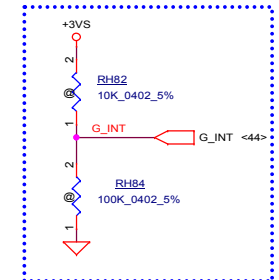
Timer system reboot feature).



VGA_ID1 / VGA_ID2 / Project_ID0 / Project_ID1 SW set GPI interanl pull down 20K.

VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
N17P-G0	0	0
N17P-G1	0	1
*N17E-G1	1	0
Reserved	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
C5MMH	0	0
*C5PRH	0	1
Reserved	1	0
Reserved	1	1



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				Date: Friday, March 31, 2017	Sheet 21 of 73

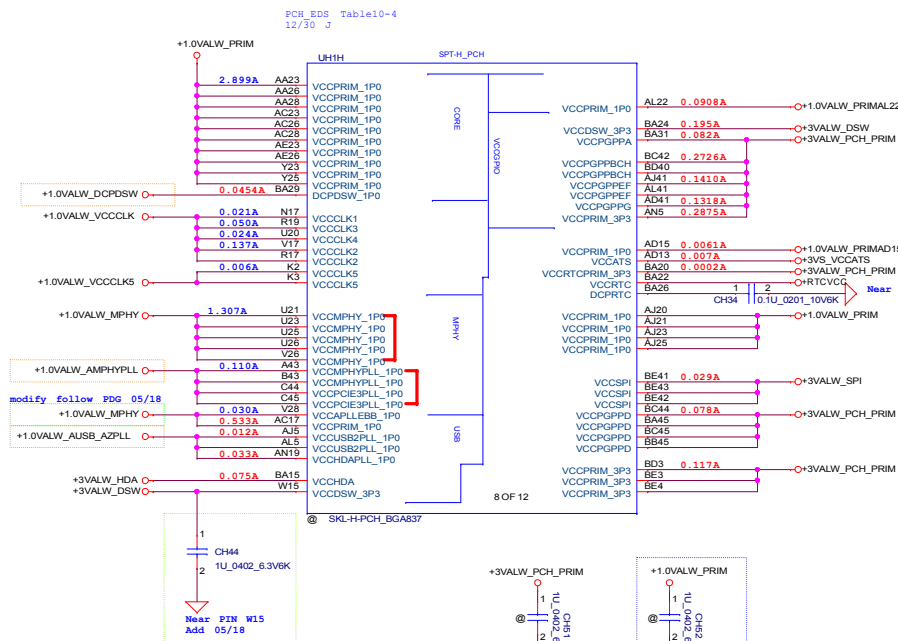
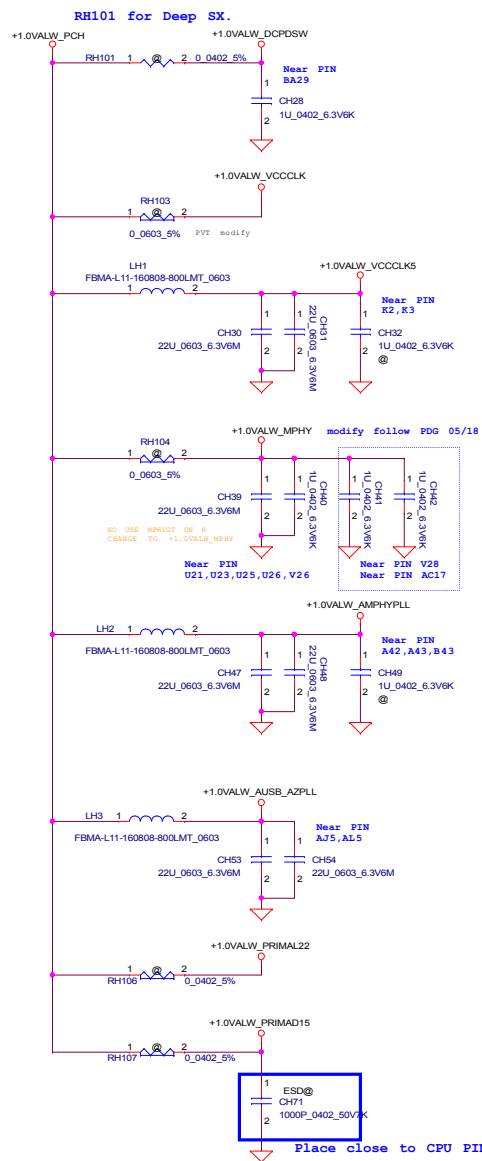
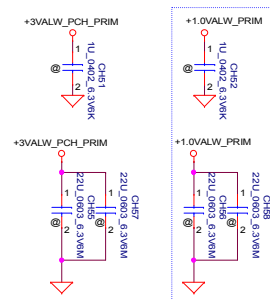
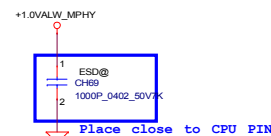


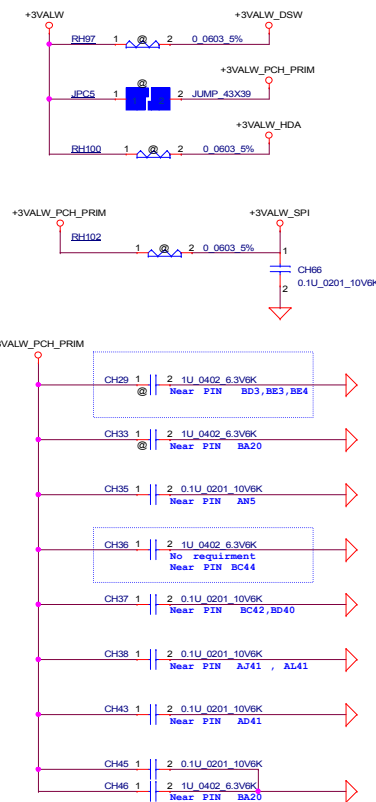
Table 10-6. PCH-H VCCMPHY 1p0 Icc Adder Per HSIO Lane

Icc (mA)	Details
700	All HSIO disabled. Assumes DMI v4 Running 100%.
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GbE Port

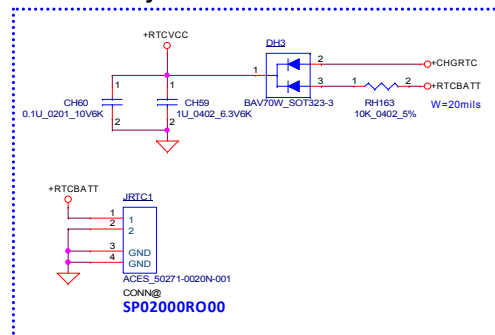
VCCMPHY power defined by HSIO lane qty.

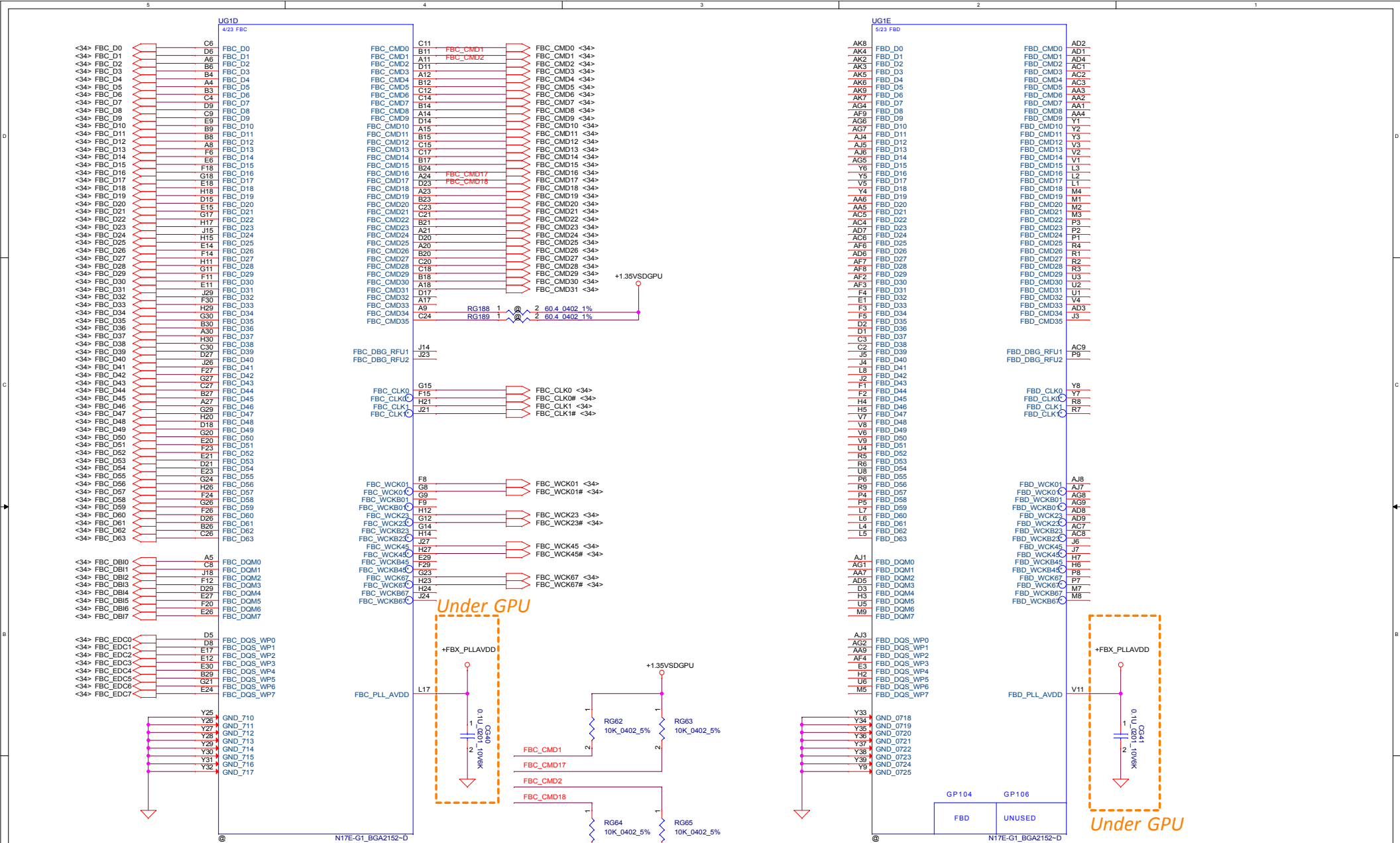


Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C (VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	



RTC Battery





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						Size		Document Number		Rev	
						C5PRH M/B LA-E921P		1A			
						Date:		Friday, March 31, 2017		Sheet 28 of 73	
						3		2		1	

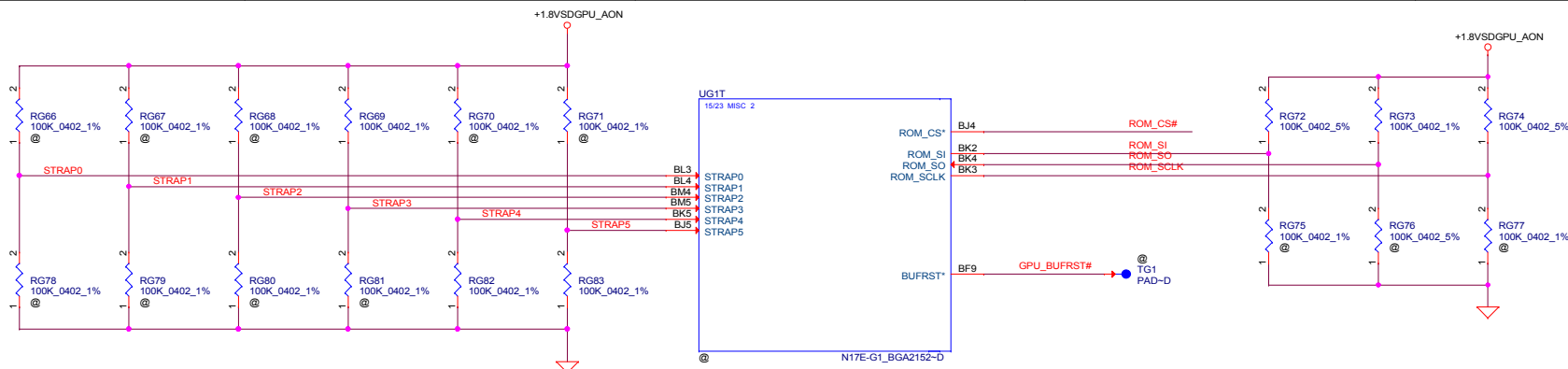


Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V ²	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V ²	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V ²	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.55V ²	Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	Full	Post production ready
		1.35V and 1.55V ²	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	Full	Post production ready

Notes:

- For N17E-G1, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
- N17E-G1 runs WCLK up to 3000 MHz with FBVDD = 1.35V. DVS is required to run WCLK > 3000 MHz.

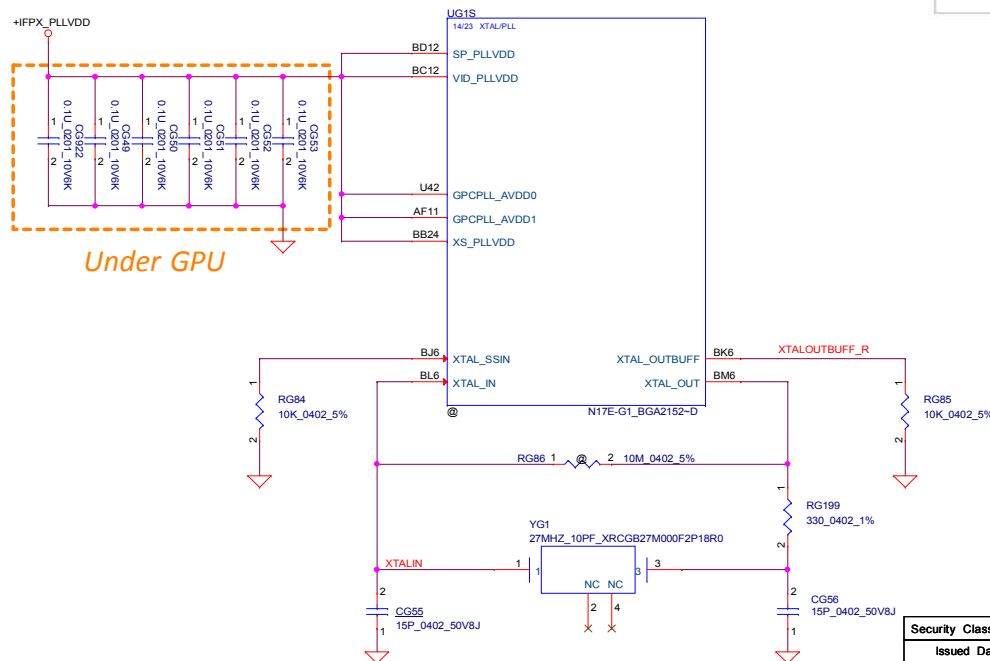
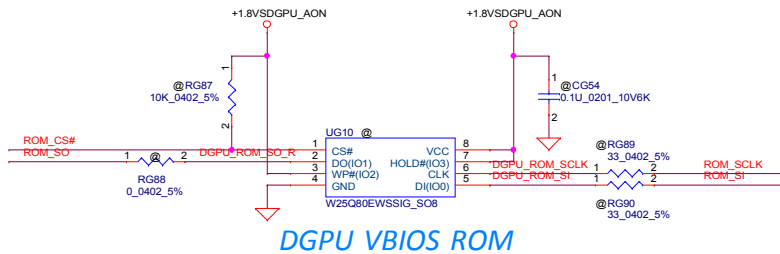
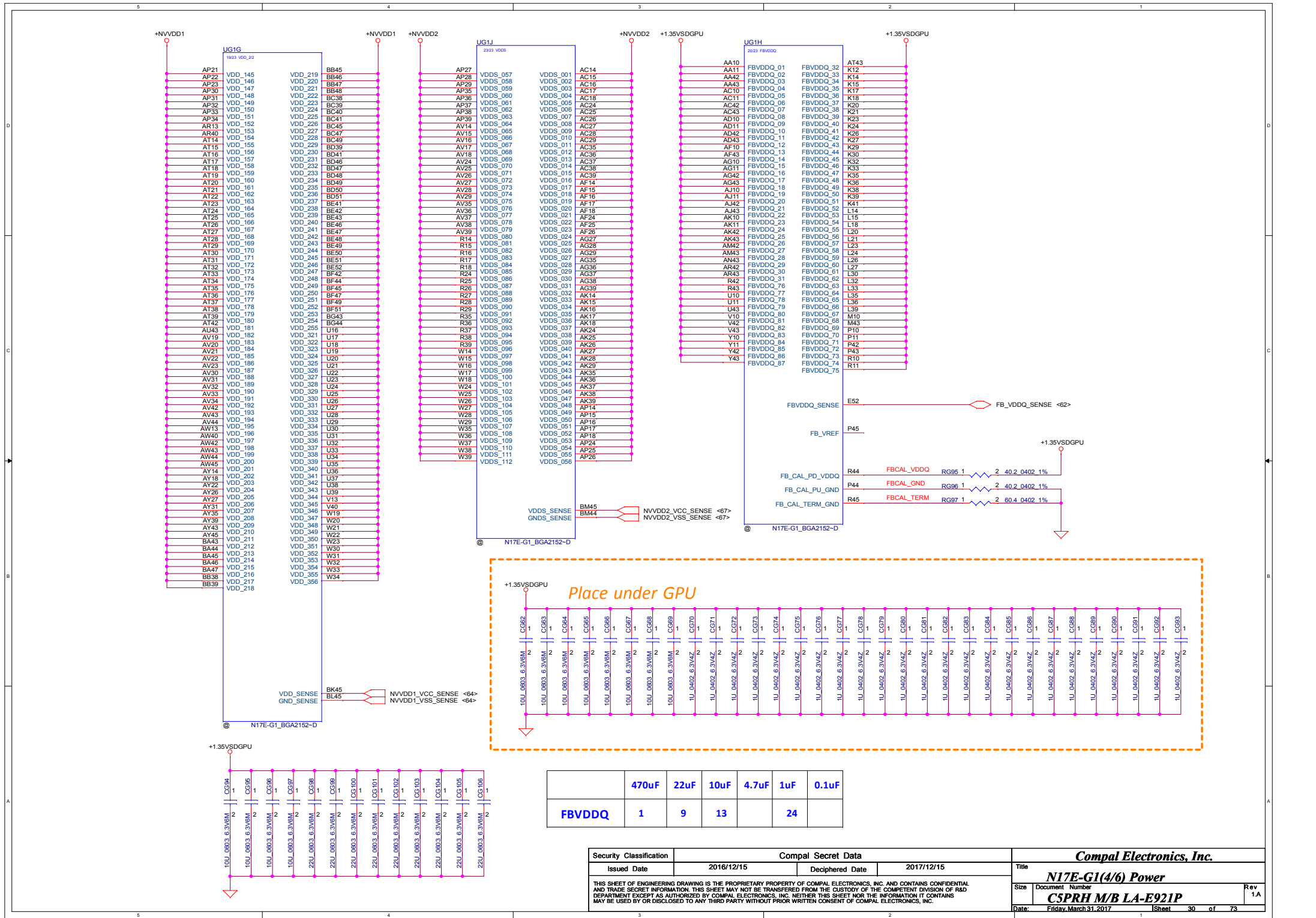
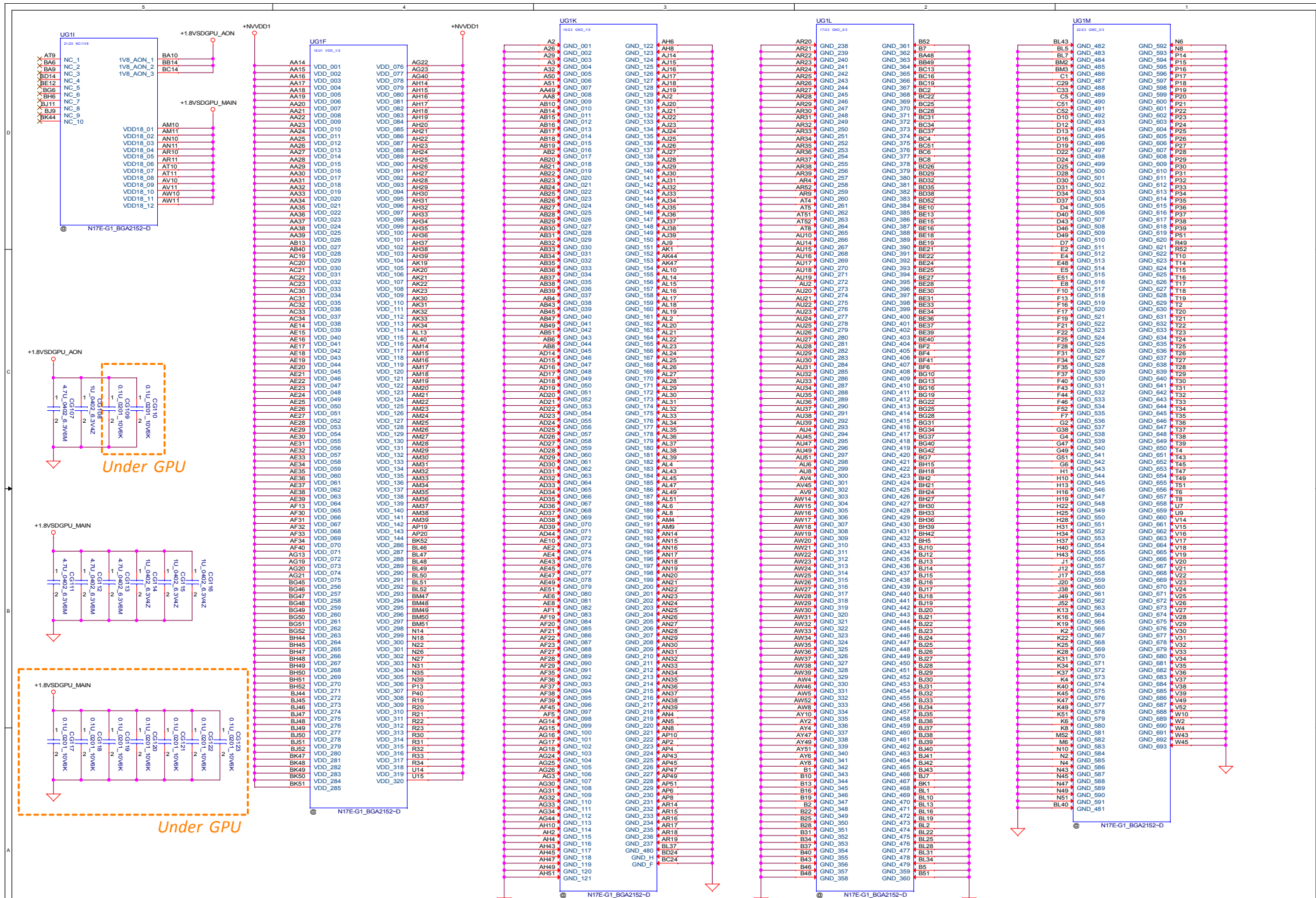


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0	(0x0000)
L	L	H	1	(0x0001)
L	H	L	2	(0x0002)
L	H	H	3	(0x0003)
H	L	L	4	(0x0004)
H	L	H	5	(0x0005)
H	H	L	6	(0x0006)
H	H	H	7	(0x0007)

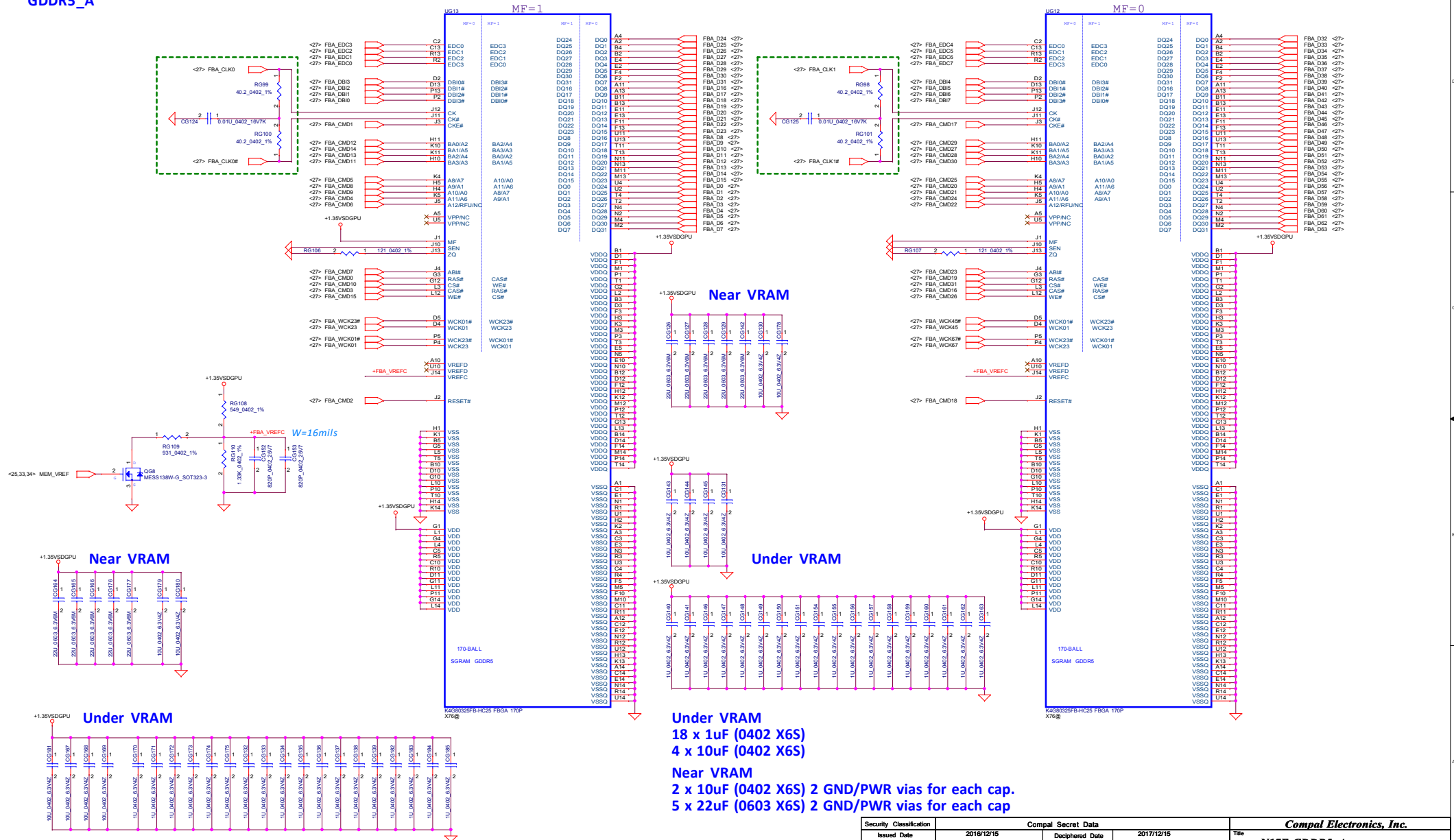
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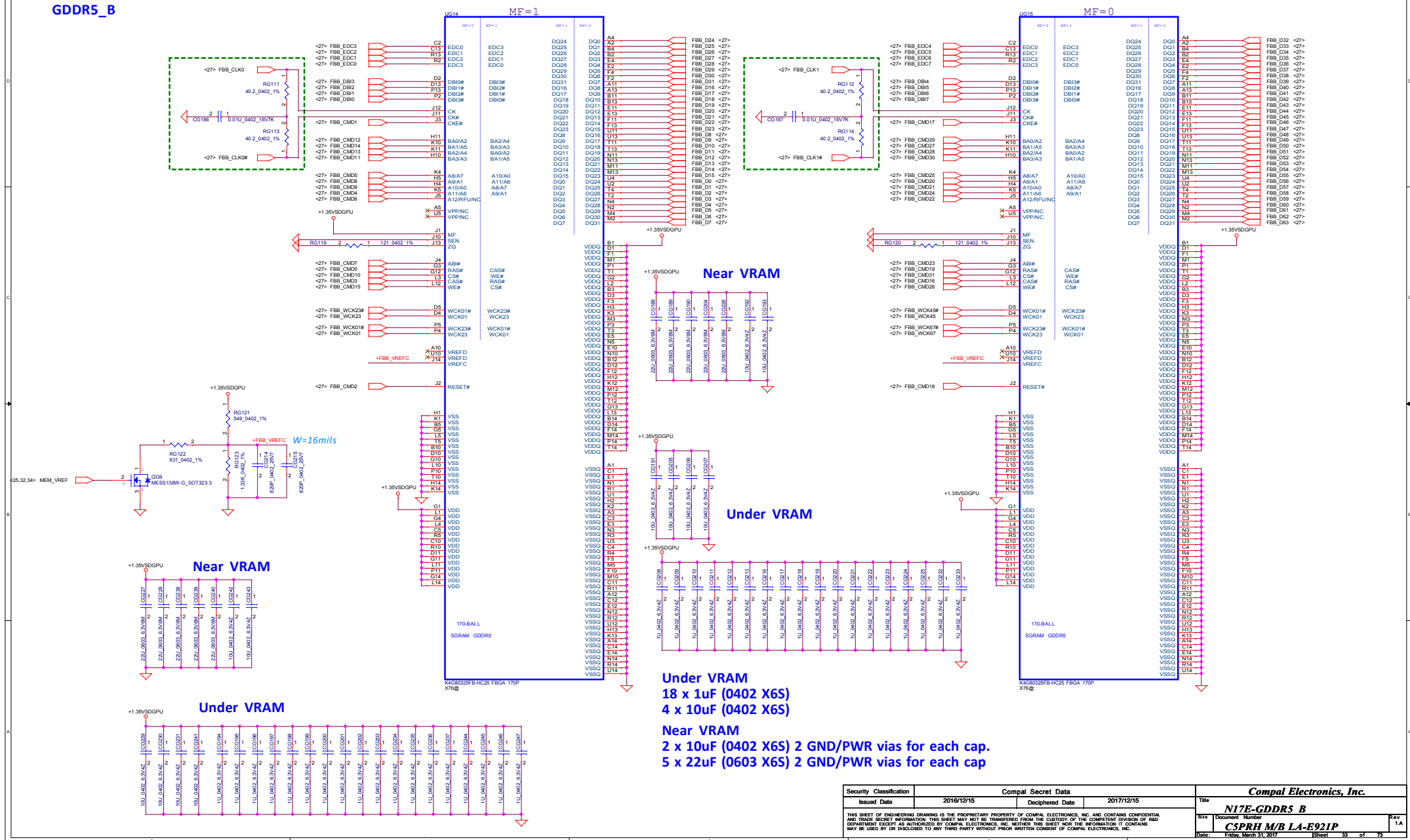
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				Size	Document Number
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GDDR5_A



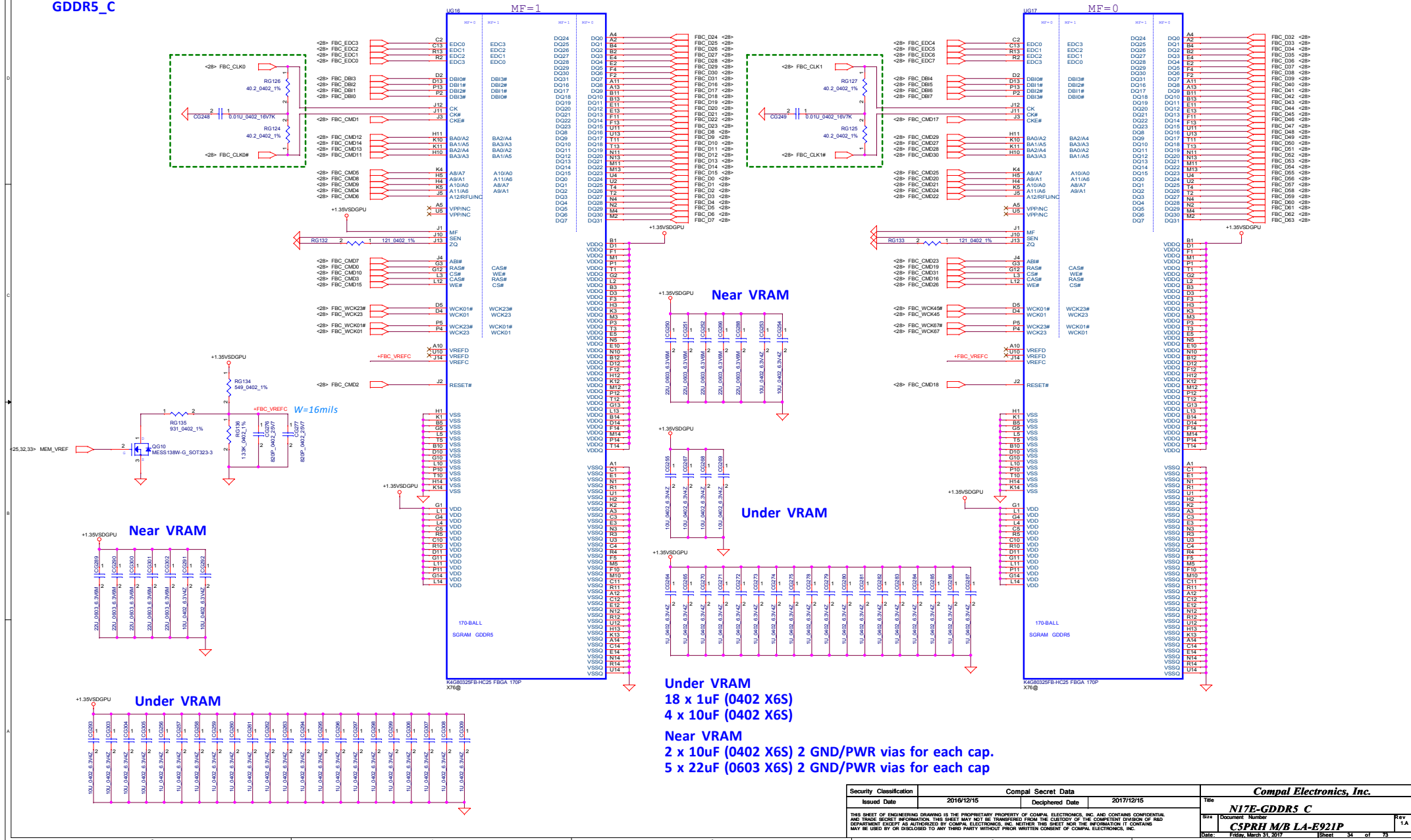
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GDDR5_B



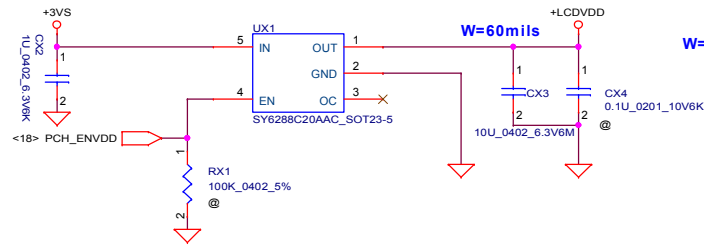
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GDDR5 C

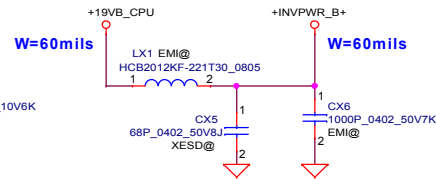


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				Sheet		34		of 73	

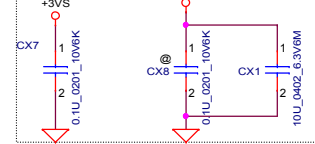
LCD POWER CIRCUIT



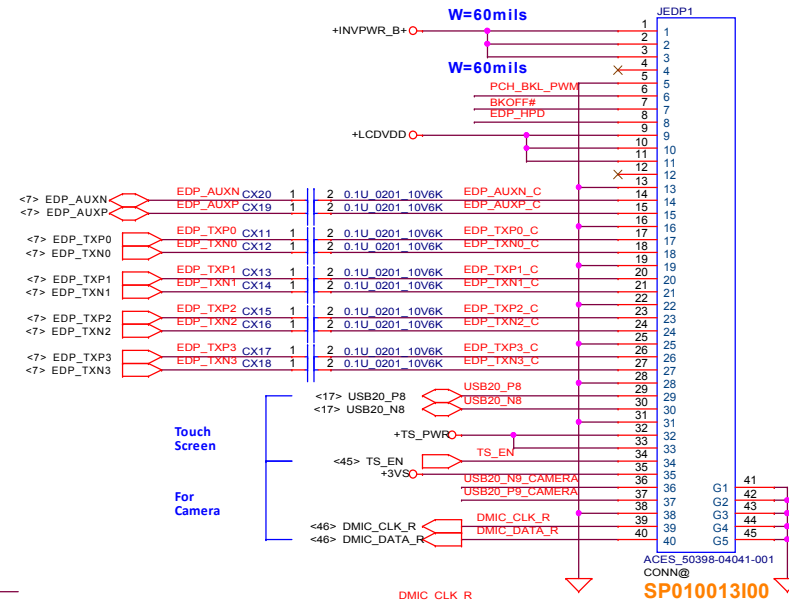
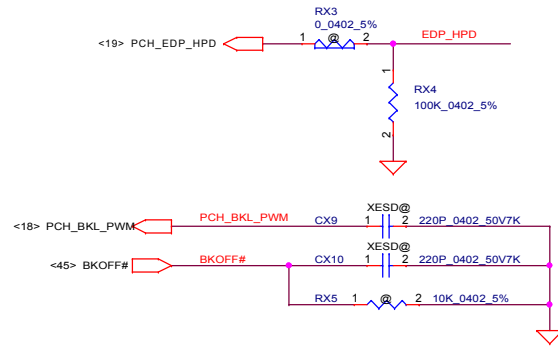
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04



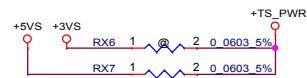
Place closed to
JEDP1



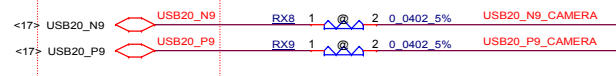
LED PANEL Conn.



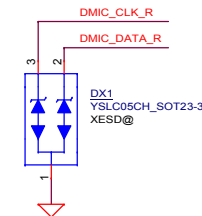
USB Touch Screen



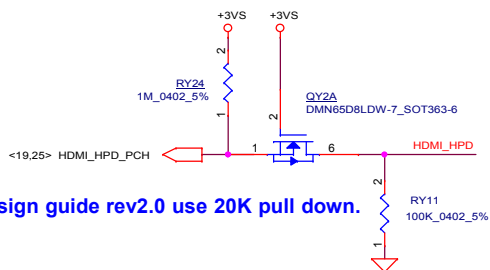
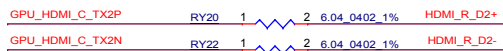
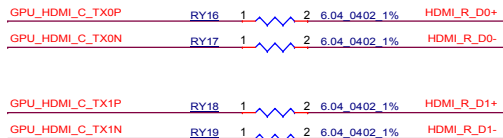
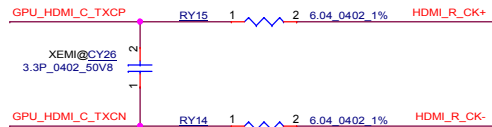
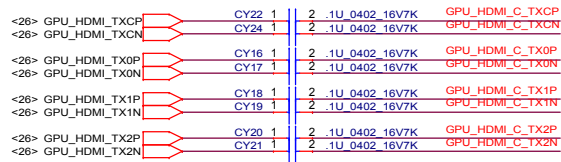
Camera



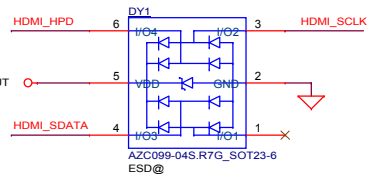
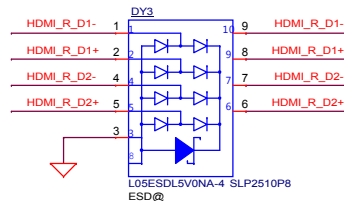
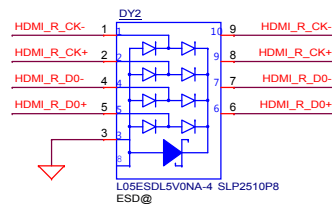
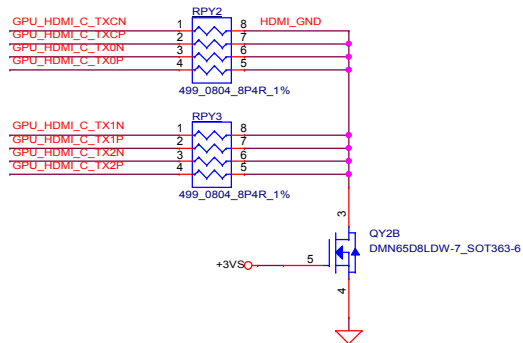
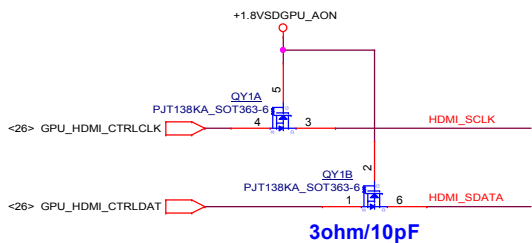
Touch Screen
For Camera



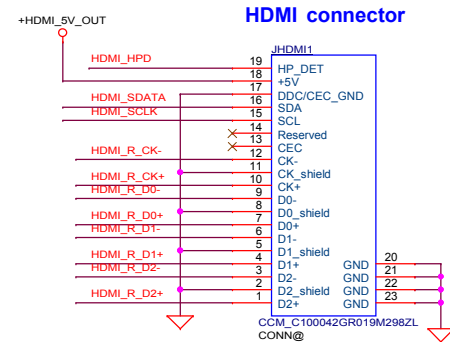
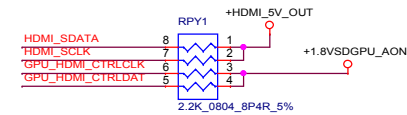
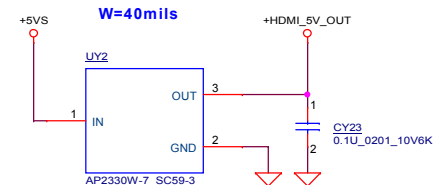
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								Size	Document Number						Rev
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RY11 design guide rev2.0 use 20K pull down.

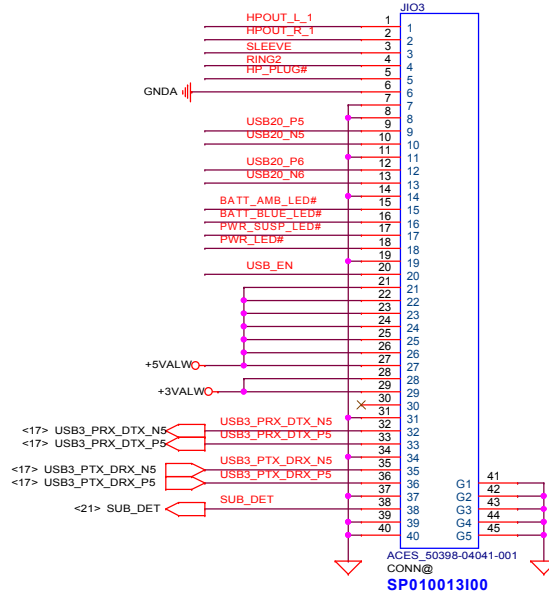
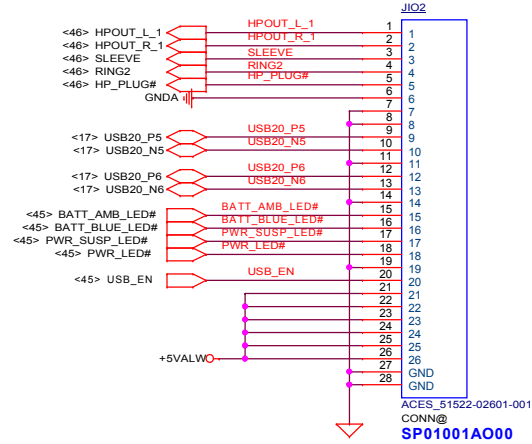


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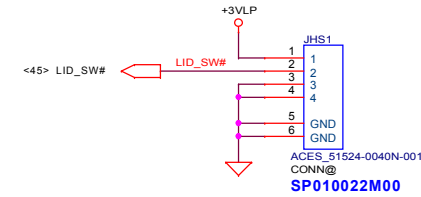


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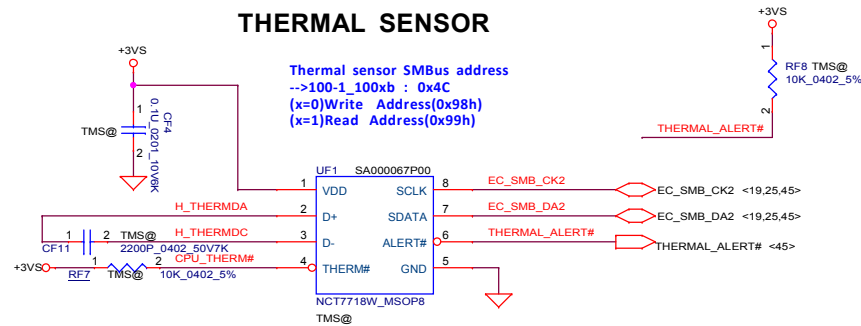
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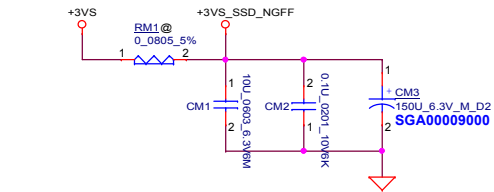
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THERMAL SENSOR



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M.2 SSD

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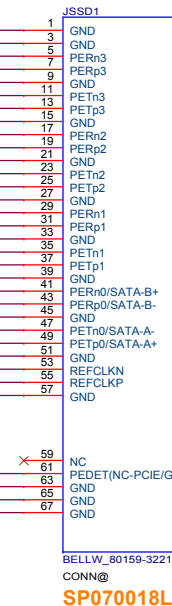
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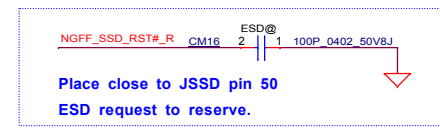
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+3VS_SSD_NGFF



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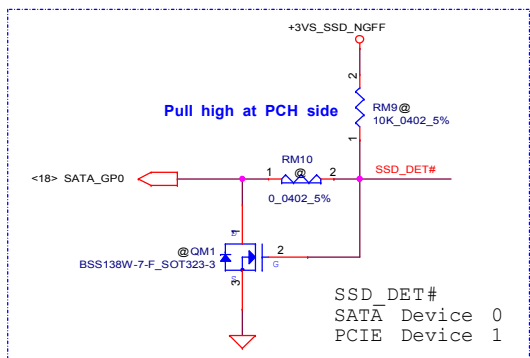
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Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

Pull high at PCH side

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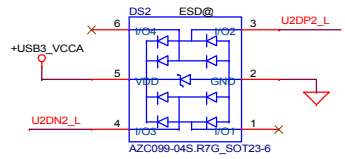
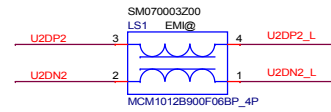
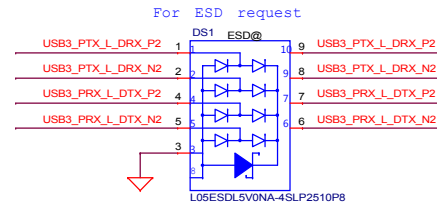
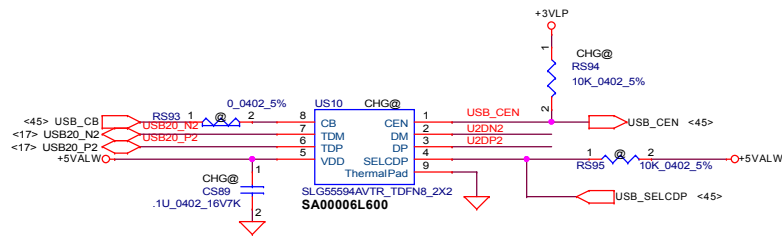
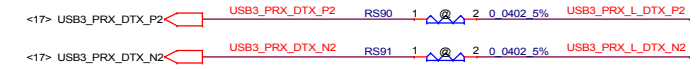
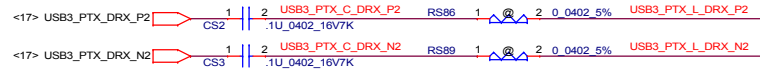
Pull high at PCH side

Pull high at PCH side

SSD_DET#
SATA Device 0
PCIE Device 1

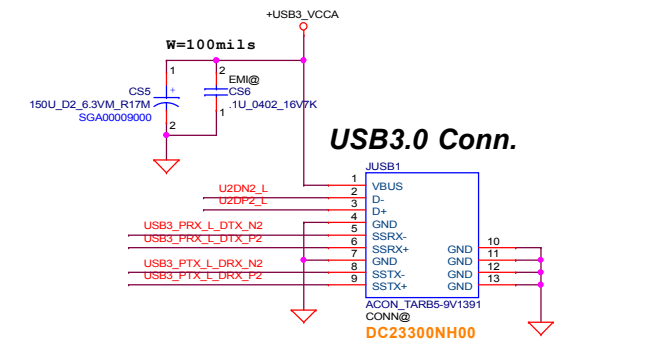
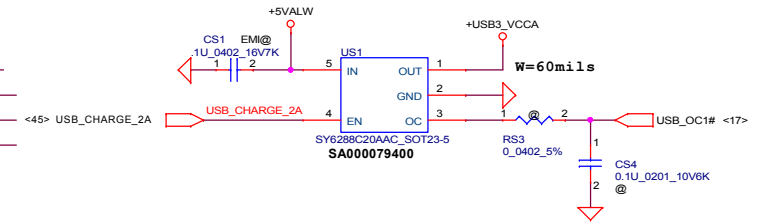
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Size	Document	Number	Rev	C5PRH M/B LA-E921P	
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USB3.0

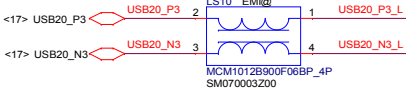
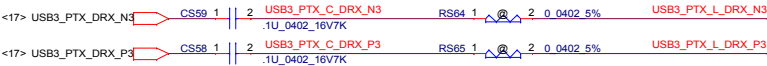


USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



USB3.0 (Port 3)

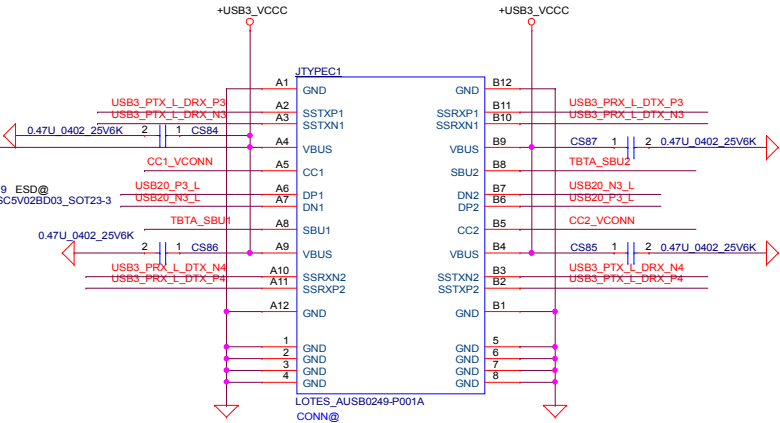
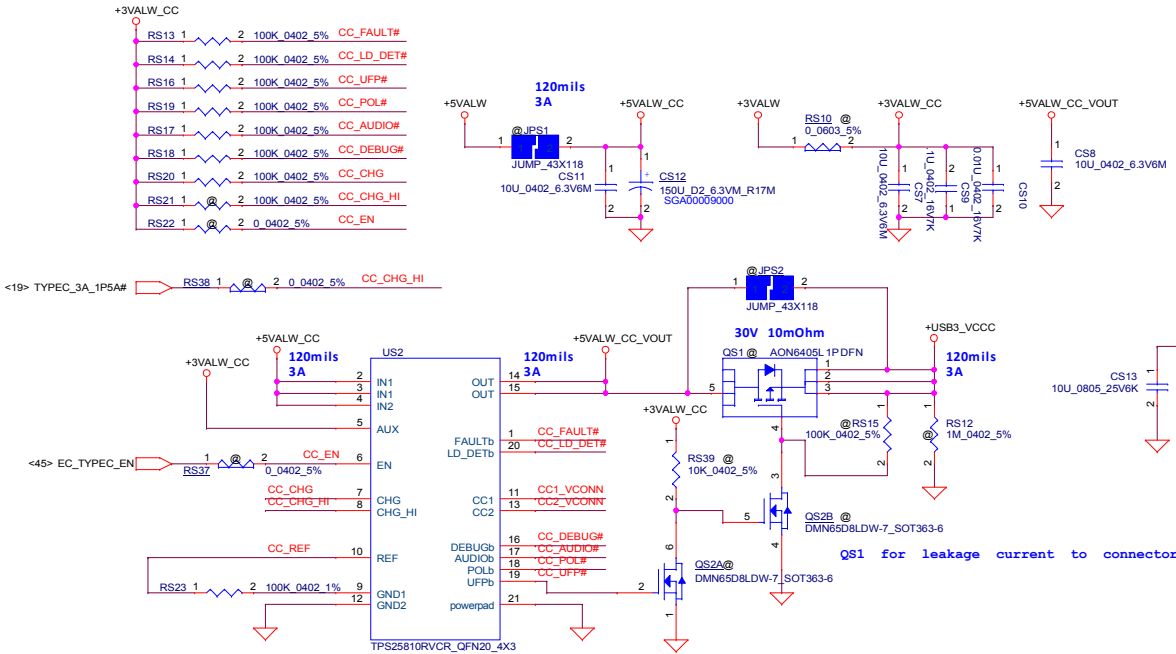
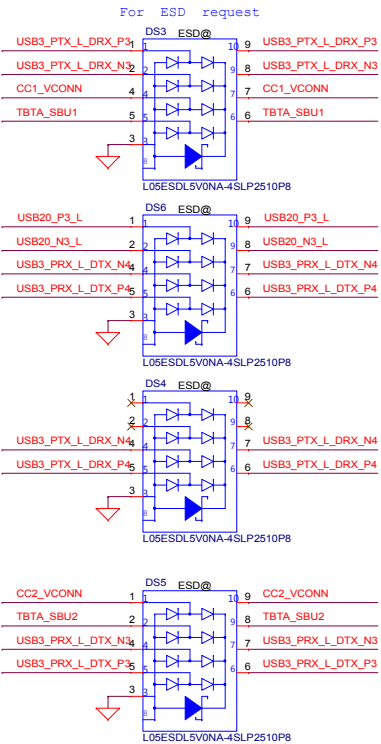


USB3.0 (Port 4)



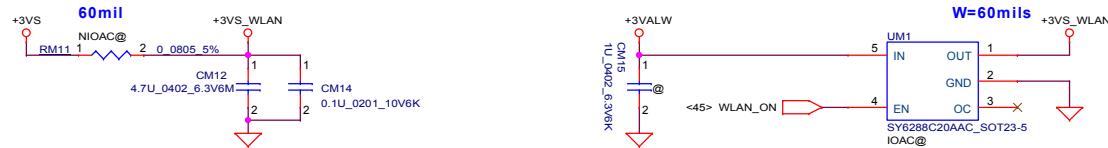
Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

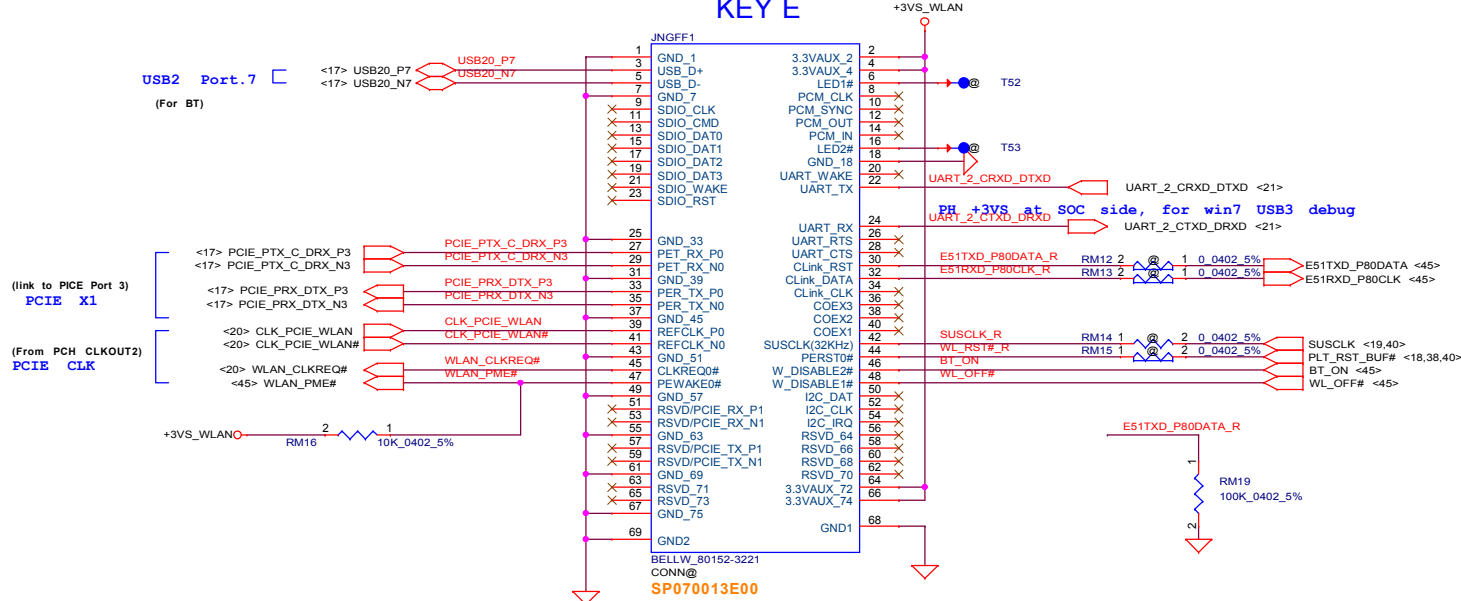


CC1_VCONN & CC2_VCONN need 20mil trace width.

Wireless LAN



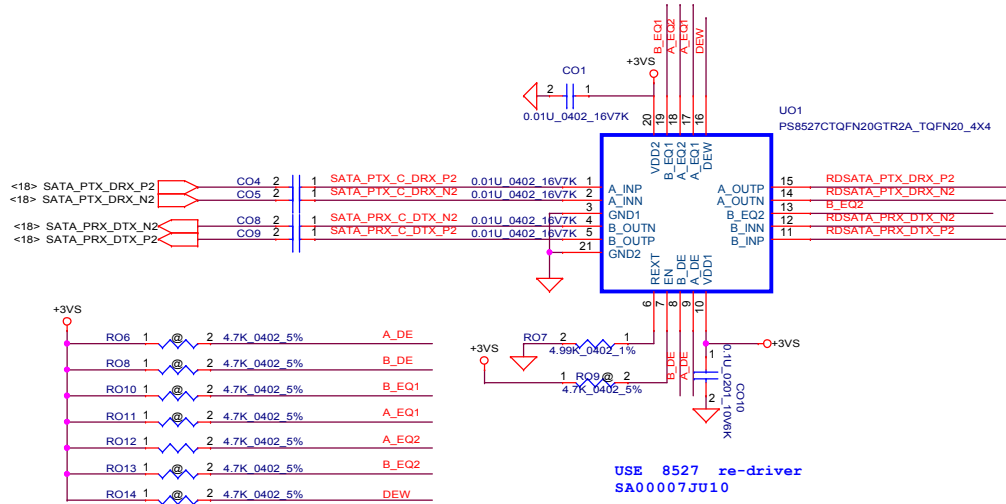
KEY E



NGFF WL+BT (KEY E)

74	I/O	GND	75
72	I/O	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/I/O/3.3)	GND	63
60	IQE CLK (IO/I/O/3.3)	Reserved/PERn1	61
58	IQE DATA (IO/I/O/3.3)	Reserved/PERp1	59
56	W_DISABLE#1 (IO/I/O/3.3V)	GND	57
54	Reserved/W_DISABLE2 (IO/I/O/3.3V)	PEWake0# (IO/I/O/3.3V)	55
52	PERST0# (IO/I/O/3.3V)	CLKREQ0# (IO/I/O/3.3V)	53
50	SUSCLK1(32KHz) (IO/I/O/3.3V)	GND	51
48	CODE#1 (IO/I/O/1.8V)	REFCLKN0	49
46	CODE#2 (IO/I/O/1.8V)	REFCLKP0	47
44	CODE#3 (IO/I/O/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	PETn0	39
36	UART_RTS (IO/I/O/1.8V)	PETp0	37
34	UART_CTS (IO/I/O/1.8V)	GND	35
32	UART_TX (IO/I/O/1.8V)	GND	33
[Redacted Section]			
22	UART Rx (IO/I/O/1.8V)	SDIO Reset# (IO/I/O/1.8V)	23
20	UART Wake# (IO/I/O/3.3V)	SDIO Wake# (IO/I/O/1.8V)	21
18	GND	SDIO DAT3 (IO/I/O/1.8V)	19
16	LED#2 (I/O/I/O)	SDIO DAT2 (IO/I/O/1.8V)	17
14	PCM_OUT/125 SD_OUT (IO/I/O/1.8V)	SDIO DAT1 (IO/I/O/1.8V)	15
12	PCM_IN/125 SD_IN (IO/I/O/1.8V)	SDIO DAT0 (IO/I/O/1.8V)	13
10	PCM_SYNC/125 MS (IO/I/O/1.8V)	SDIO CMD0 (IO/I/O/1.8V)	11
8	PCM_CLK/125 SCK (IO/I/O/1.8V)	SDIO CLKIO (IO/I/O/1.8V)	9
6	LED#1 (I/O/I/O)	GND	7
4	I/O	USB_D-	5
2	I/O	USB_D+	3
		GND	1

SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10

Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

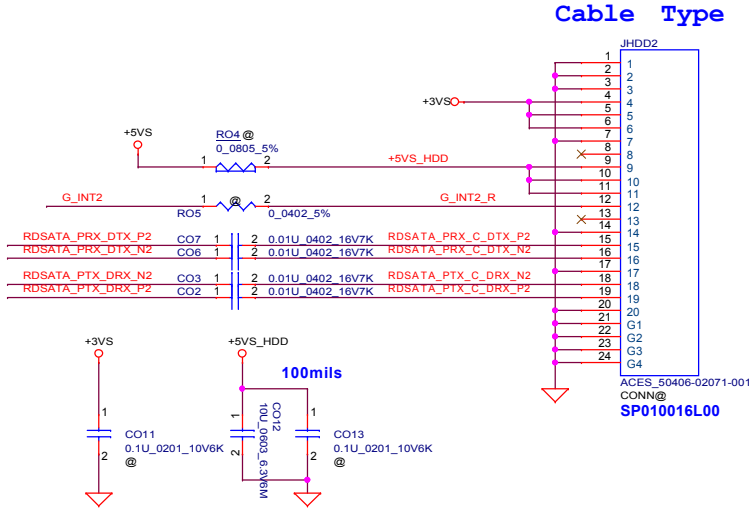
B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

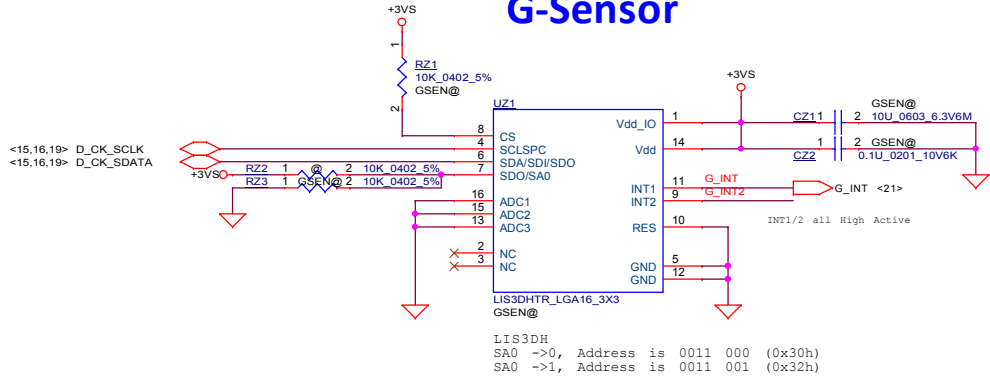
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

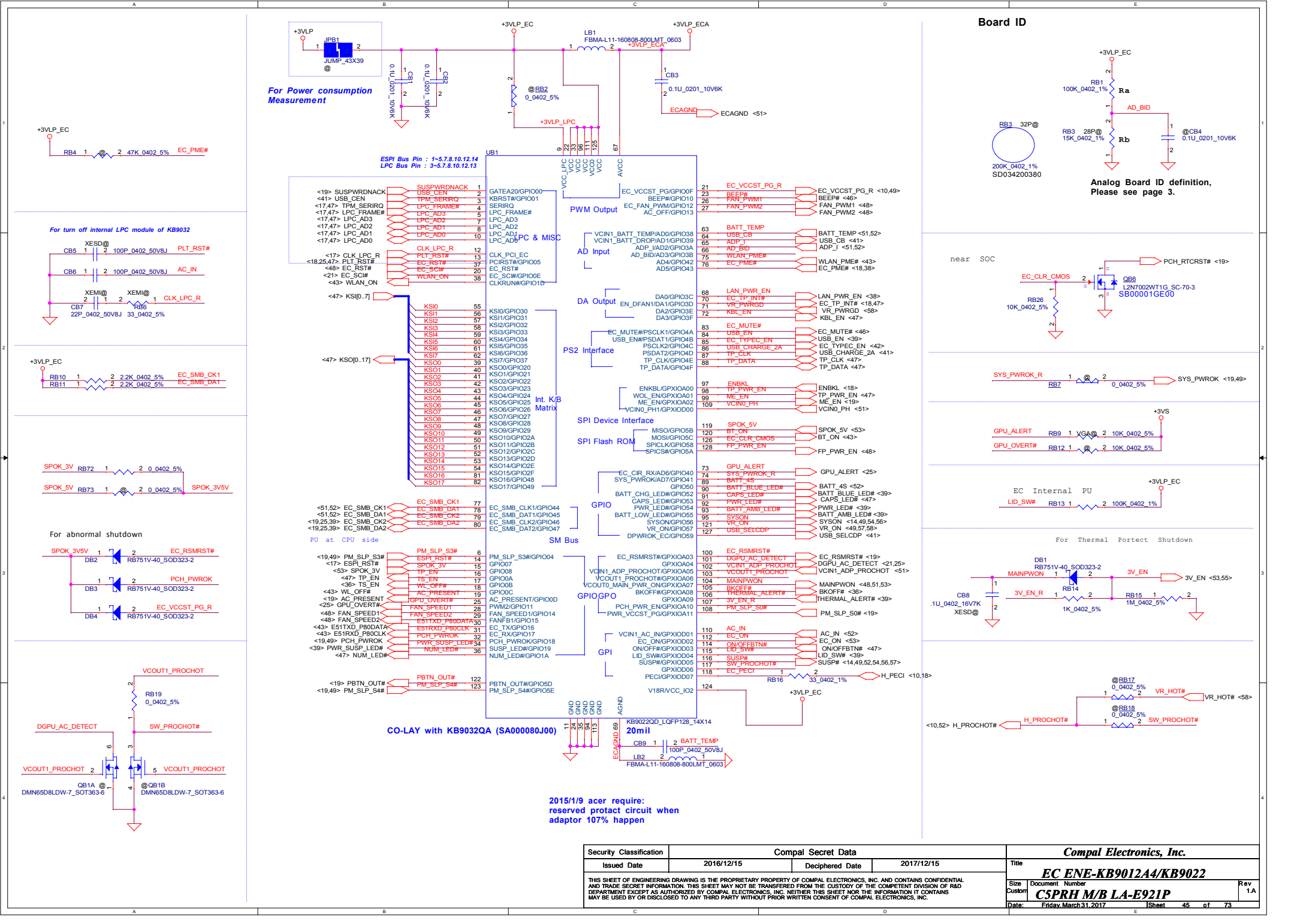
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB



G-Sensor

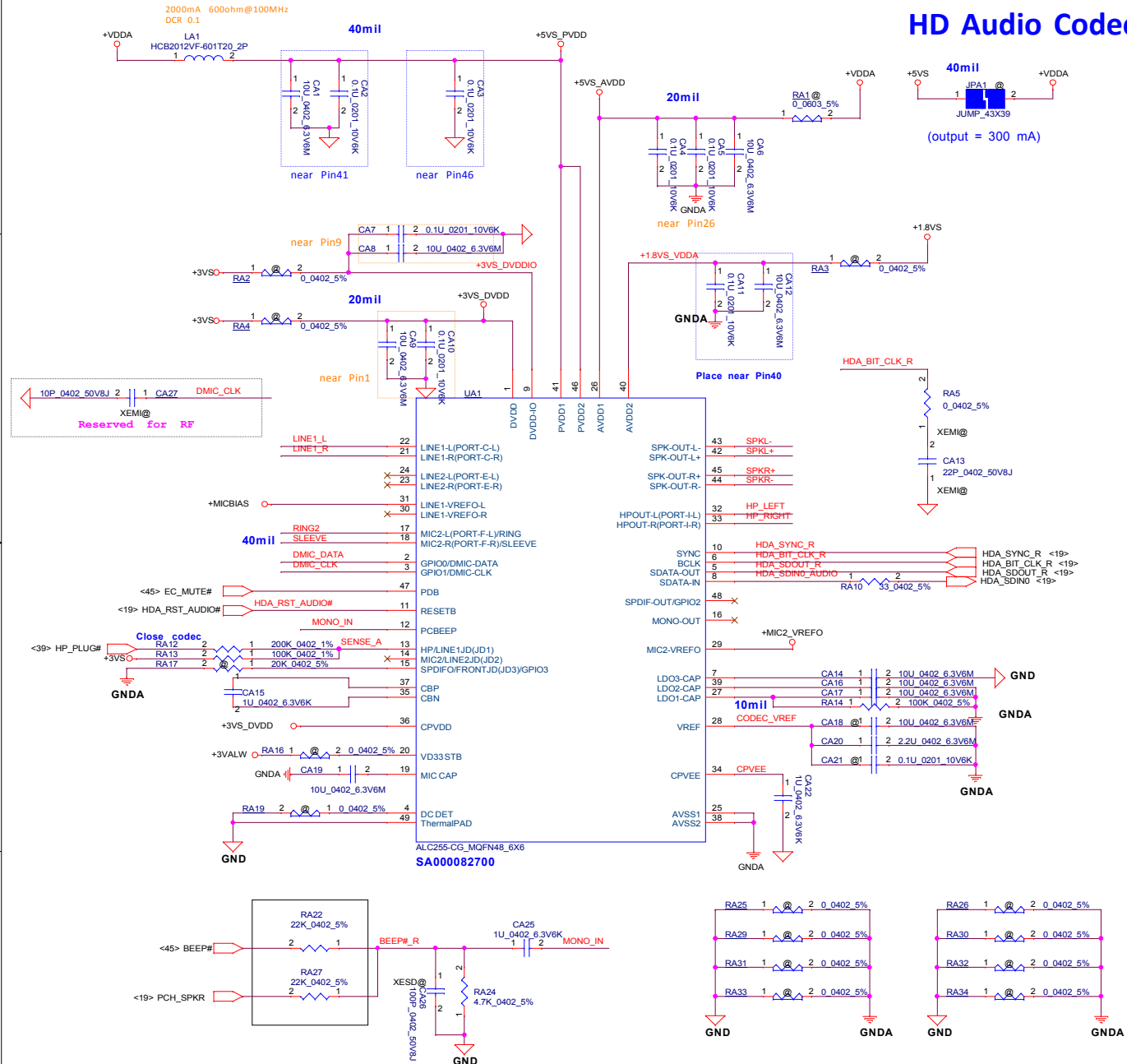




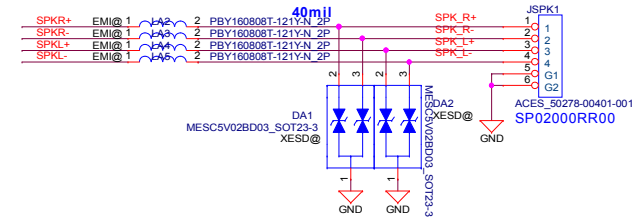
2015/1/9 acer require:
reserved protect circuit when
adaptor 107% happen

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HD Audio Codec

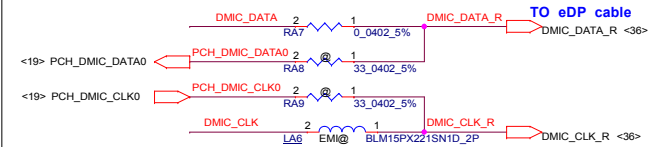


Int. Speaker Conn.

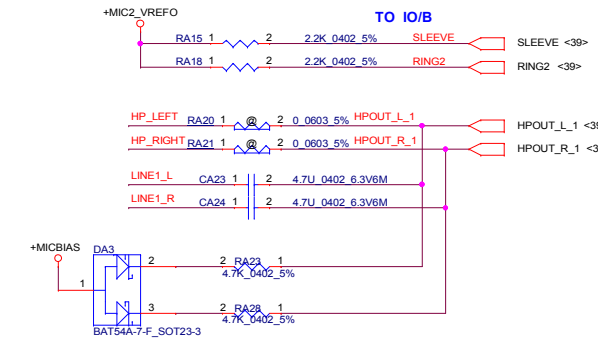


Digital MIC

MIC BOM upload by Audio Team

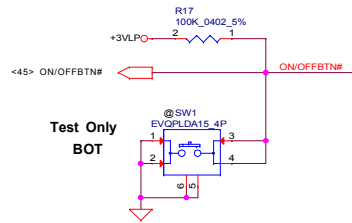


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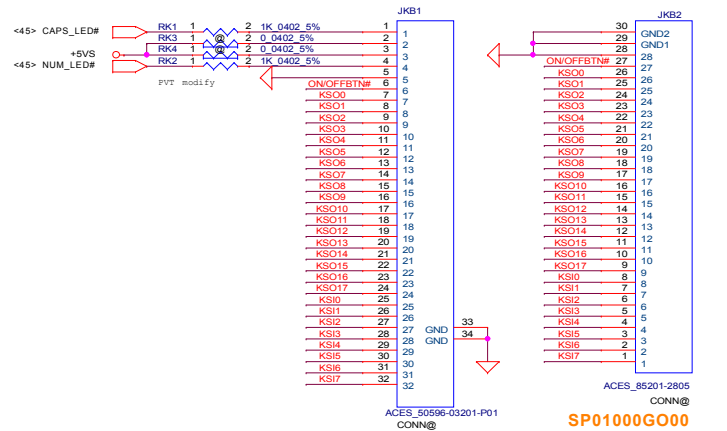


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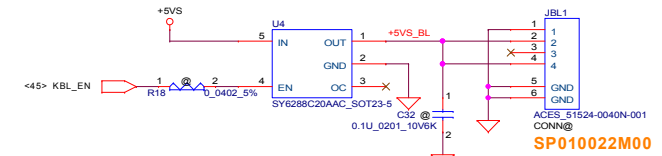
ON/OFF BTN



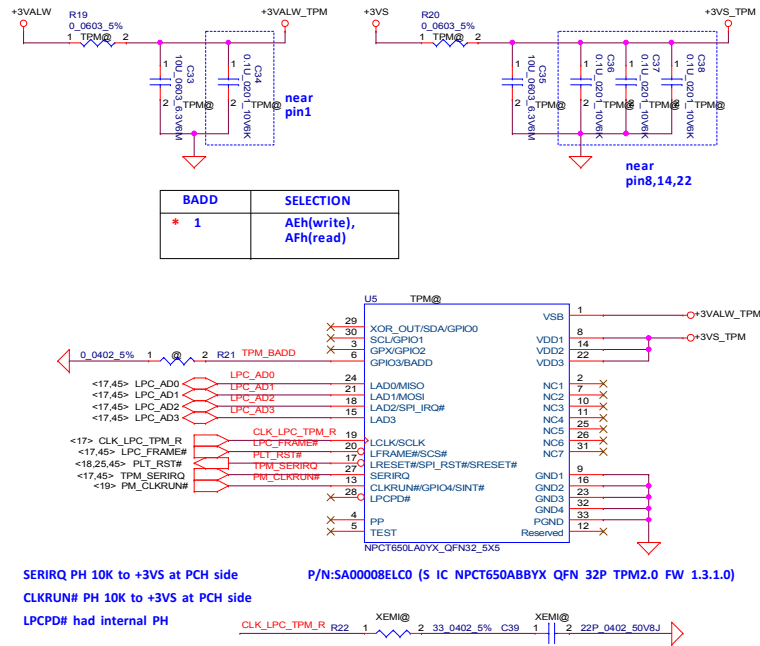
KB Conn.



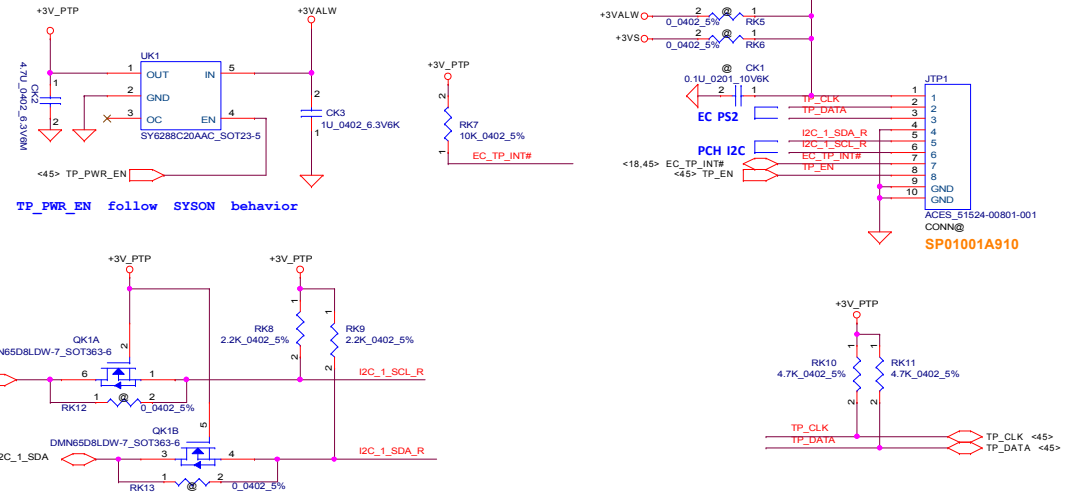
KB BackLight



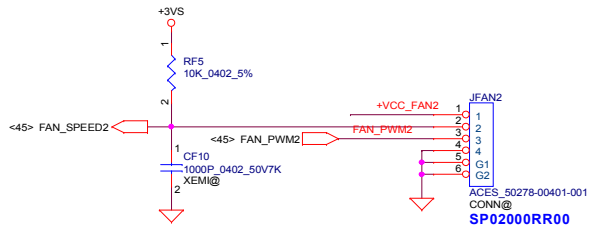
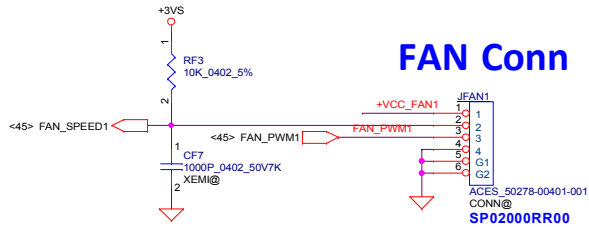
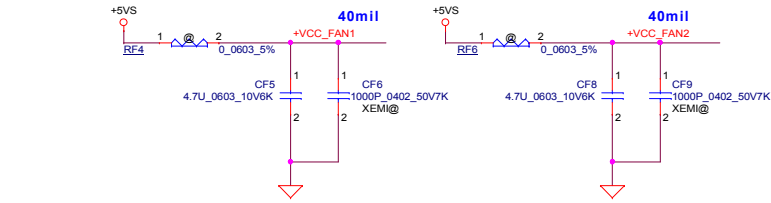
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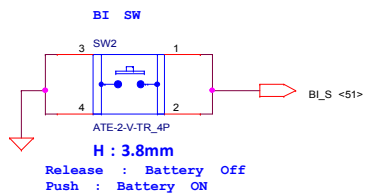
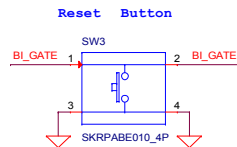
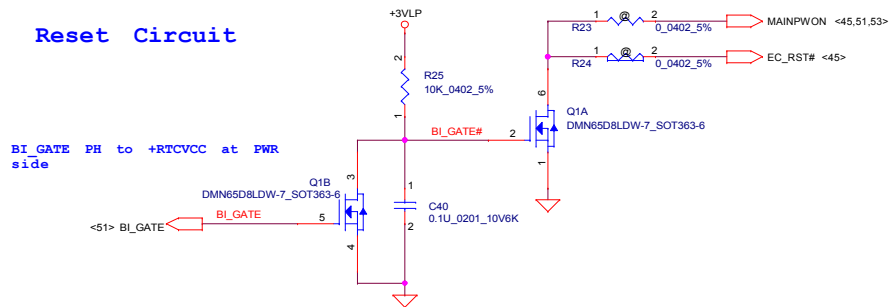
Touch Pad



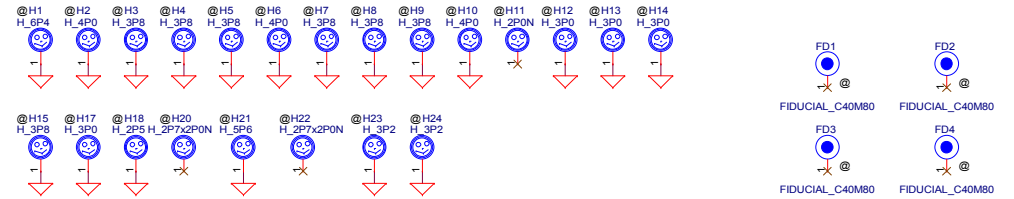
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Issued Date	2016/12/15	Deciphered Date	2017/12/15	KB & TP & TPM Connector	
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				Date:	Friday, March 31, 2017
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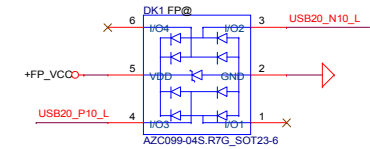
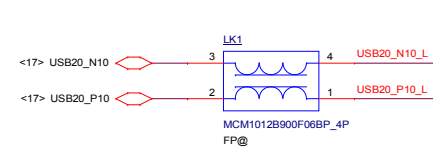
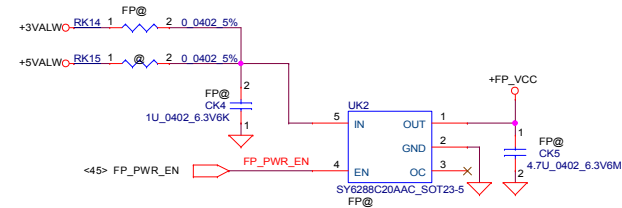
Reset Circuit



Screw Hole



Finger Print

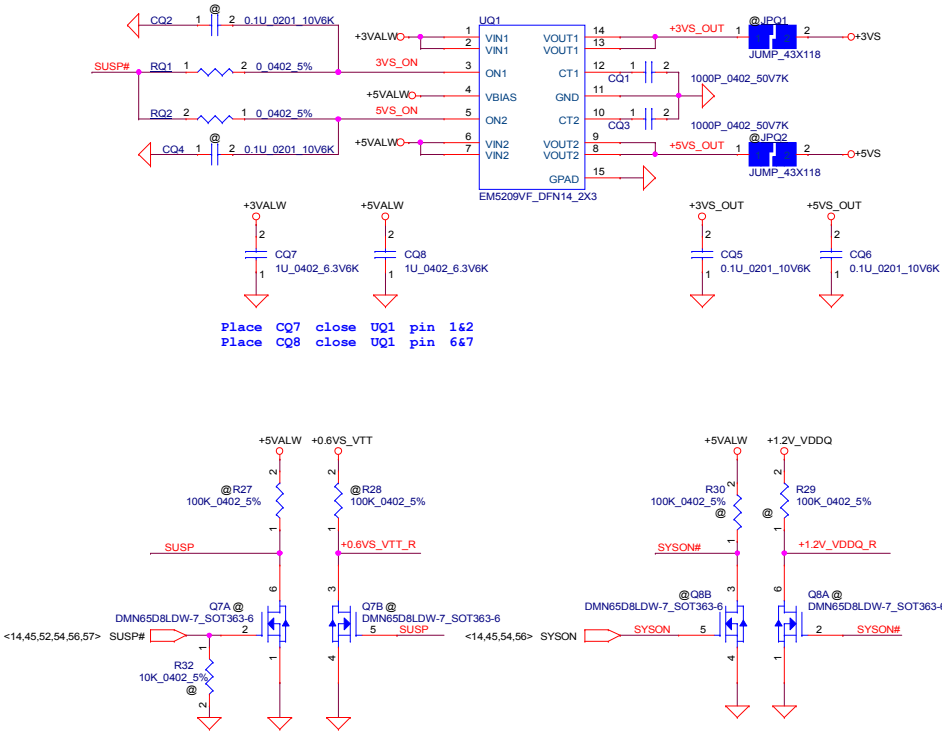


PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

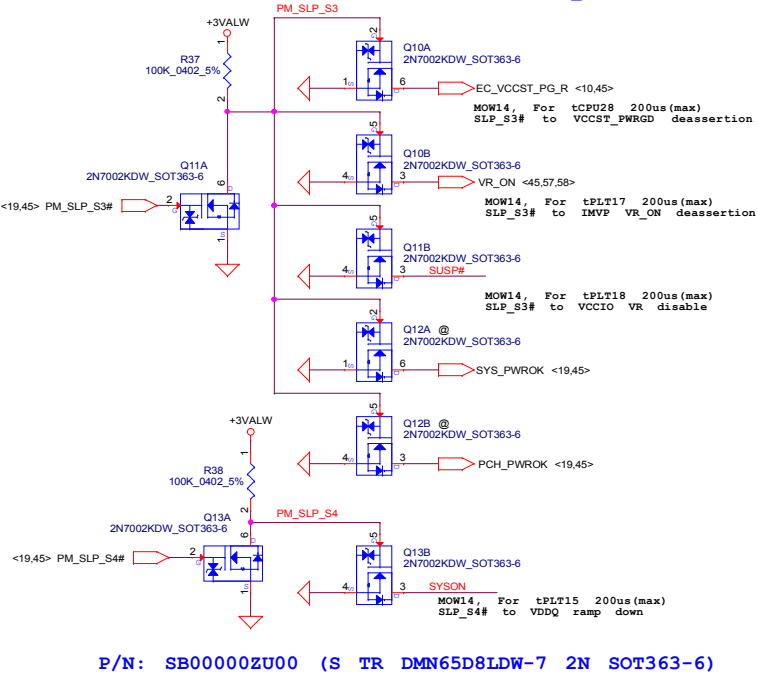
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2016/12/15				2017/12/15			
Deciphered Date											
Title				FAN & FP & Screw Hole				CSPRH M/B LA-E921P			
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Custort											
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System DC interface



For Power ON/Off Sequence



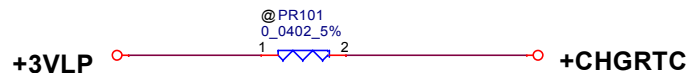
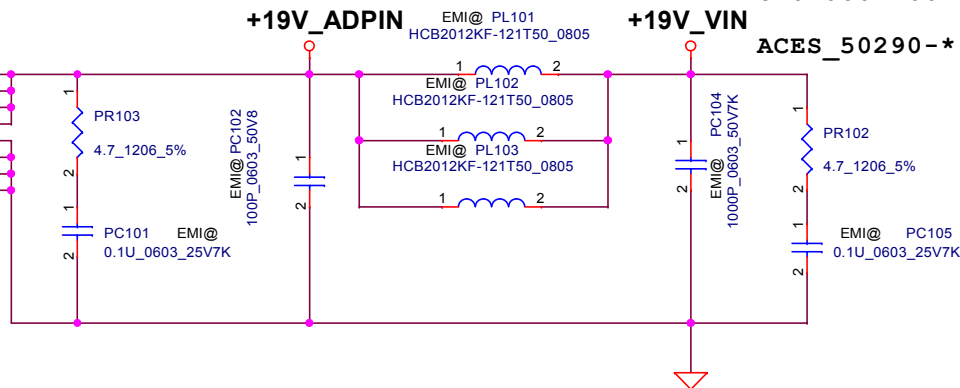
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		Custom		1A	
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		Sheet		49 of 73	

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ACES_50290-00801-001



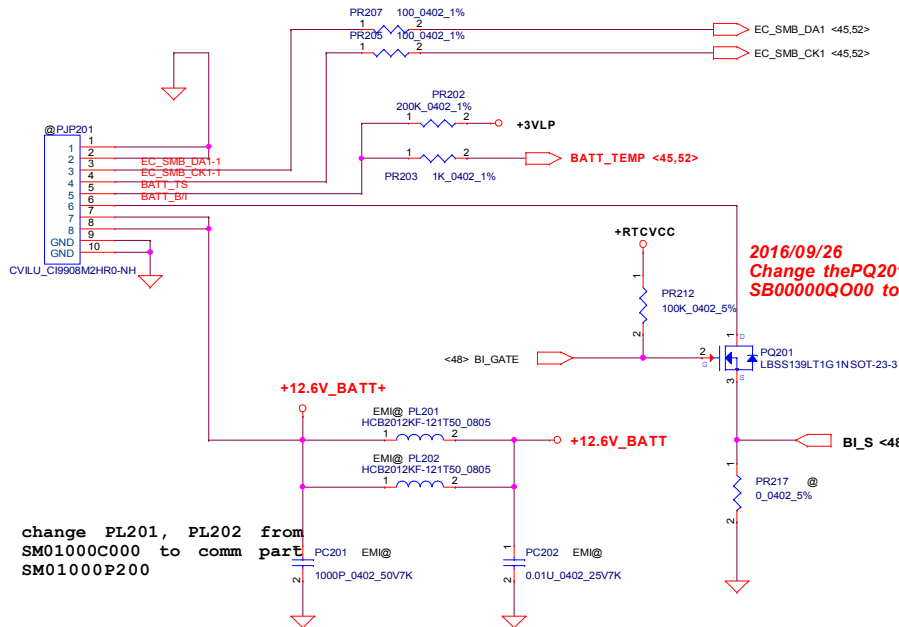
PJP101
99.9



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Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

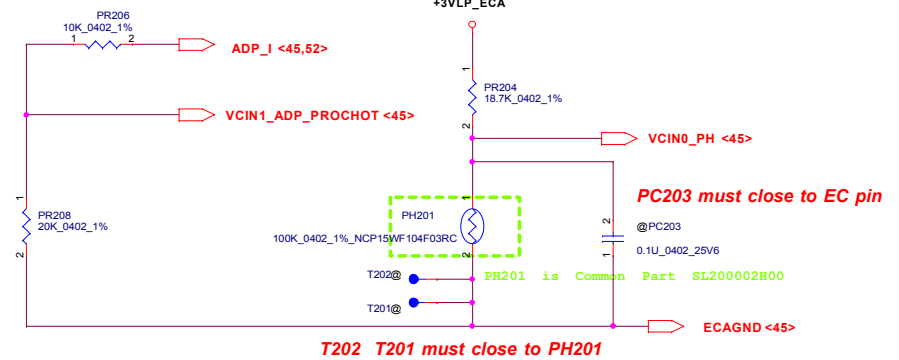


2016/11/22 update

For KB9022 sense 5mΩ	Active	Recovery
180W PR206 10K ohm	234W, 0.82V	

When PR204=16.9K

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92'C, 1V	56'C, 2V
PH202 (ohm)	7.3092K	26.11K



$$ADP_I = 20 * I(\text{adapter}) * 0.01$$

$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$

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Check pull up resistor of SPOK at HW side

EN1 and EN2 don't floating

Choke 1.5uH SH000016800 (Common Part)
(Size:4.9 x 5.2 x 3 mm)
(DCR:20m~25m)

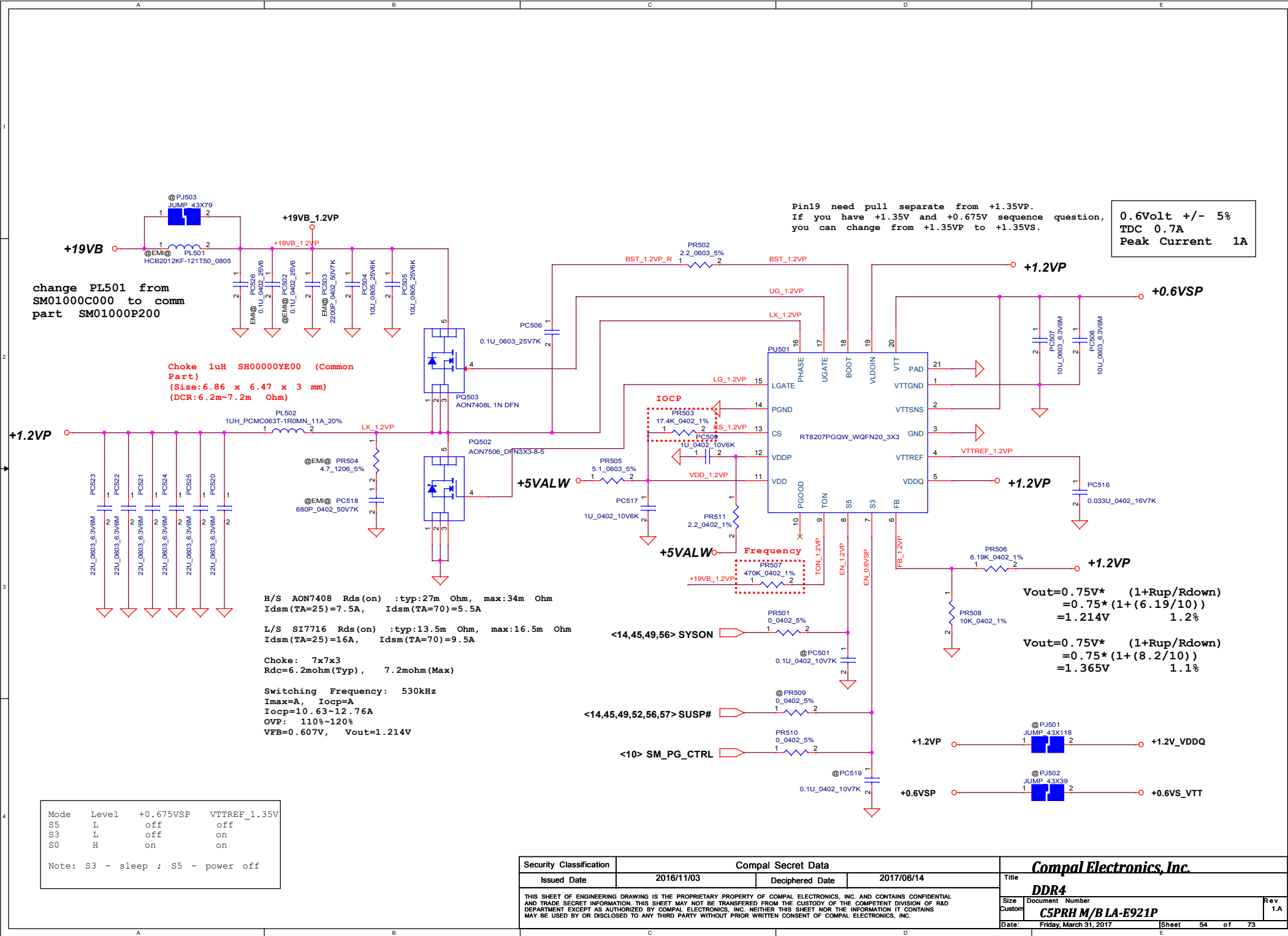
Vout is 3.234V~3.366V
Ipeak=4.65A
Imax=3.25A
Iocp=10A

Choke 1.5uH SH000016700 (Common Part)
(Size:7.3 x 6.6 x 3 mm)
(DCR:14m~15m)

Vout is 4.998V~5.202V
Ipeak=9A
Imax=6.6A
Iocp=10A

<45> EC_ON
<45,48,51> MAINPWON

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change PL501 from
SM01000C000 to comm
part SM01000P200

Choke 1uH SH00000YE00 (Common
Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)

H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A
L/S SI7716 Rds(on) :typ:13.5m Ohm, max:16.5m Ohm
Idsm(TA=25)=16A, Idsm(TA=70)=9.5A
Choke: 7x7x3
Rdc=6.2mohm(Typ), 7.2mohm(Max)
Switching Frequency: 530kHz
Imax=A, Iocp=A
Iocp=10.63~12.76A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

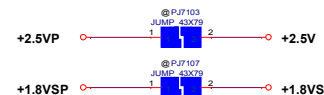
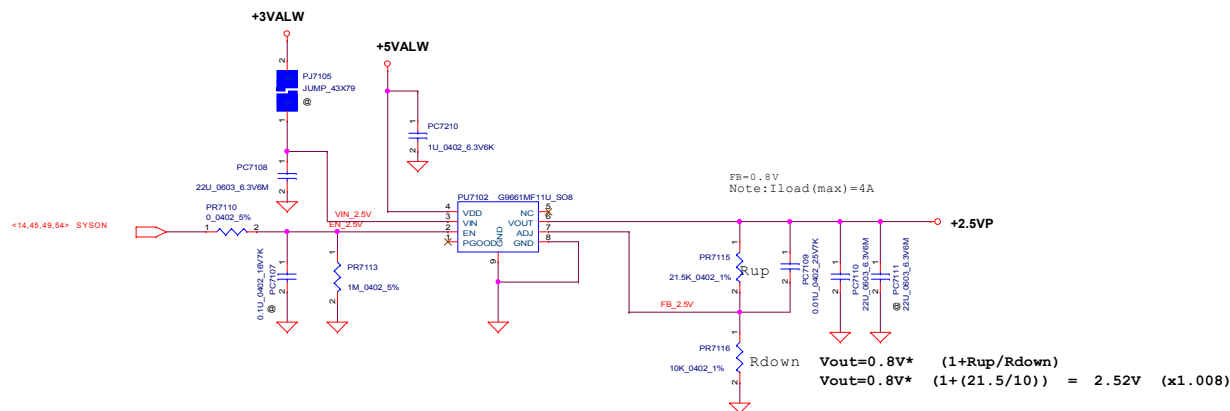
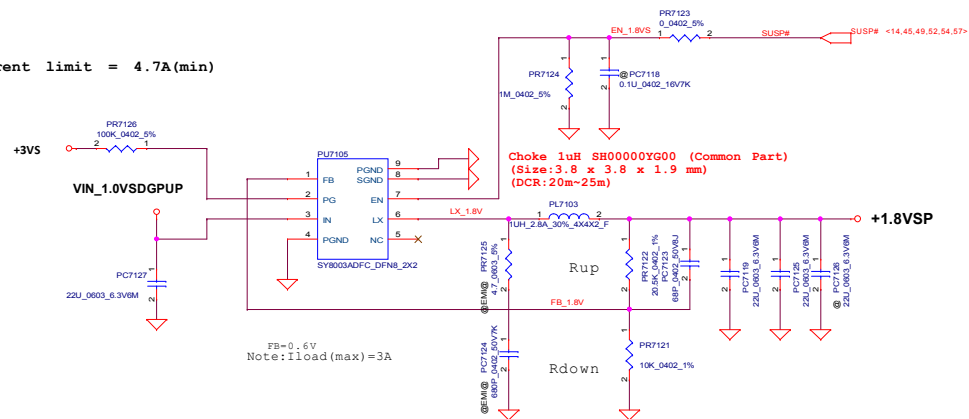
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

$$V_{out}=0.75V \cdot \left(1 + \frac{R_{up}}{R_{down}}\right) = 0.75V \cdot \left(1 + \frac{6.19}{10}\right) = 1.214V \quad 1.2\%$$
$$V_{out}=0.75V \cdot \left(1 + \frac{R_{up}}{R_{down}}\right) = 0.75V \cdot \left(1 + \frac{8.2}{10}\right) = 1.365V \quad 1.1\%$$

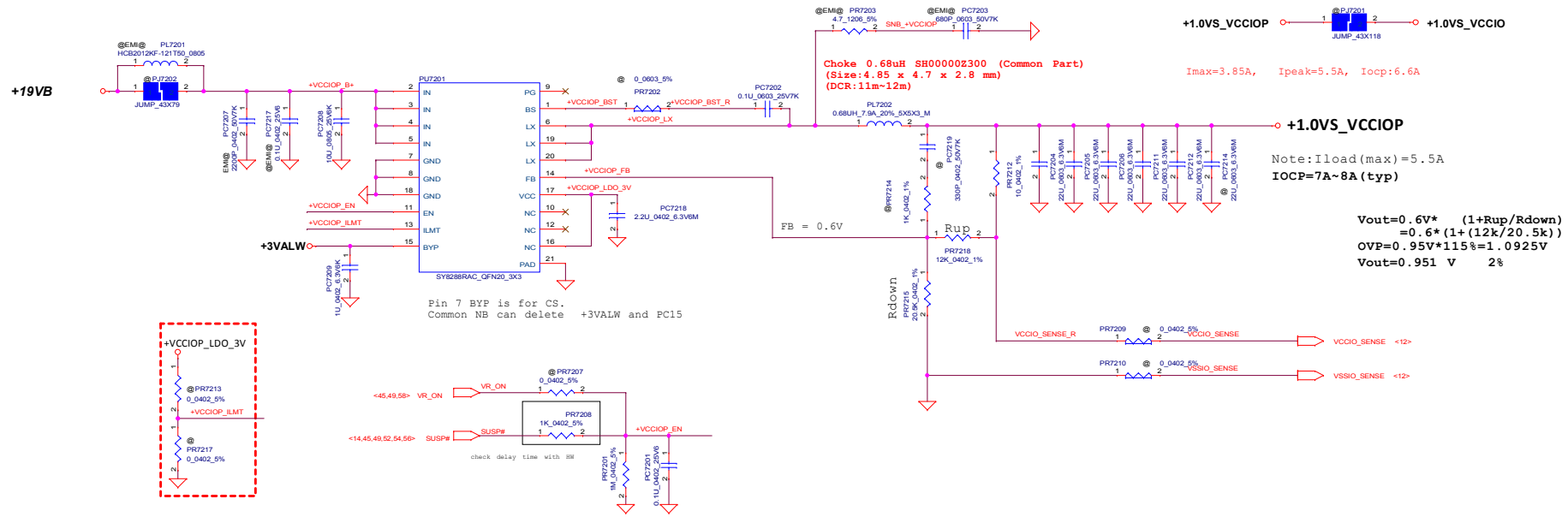
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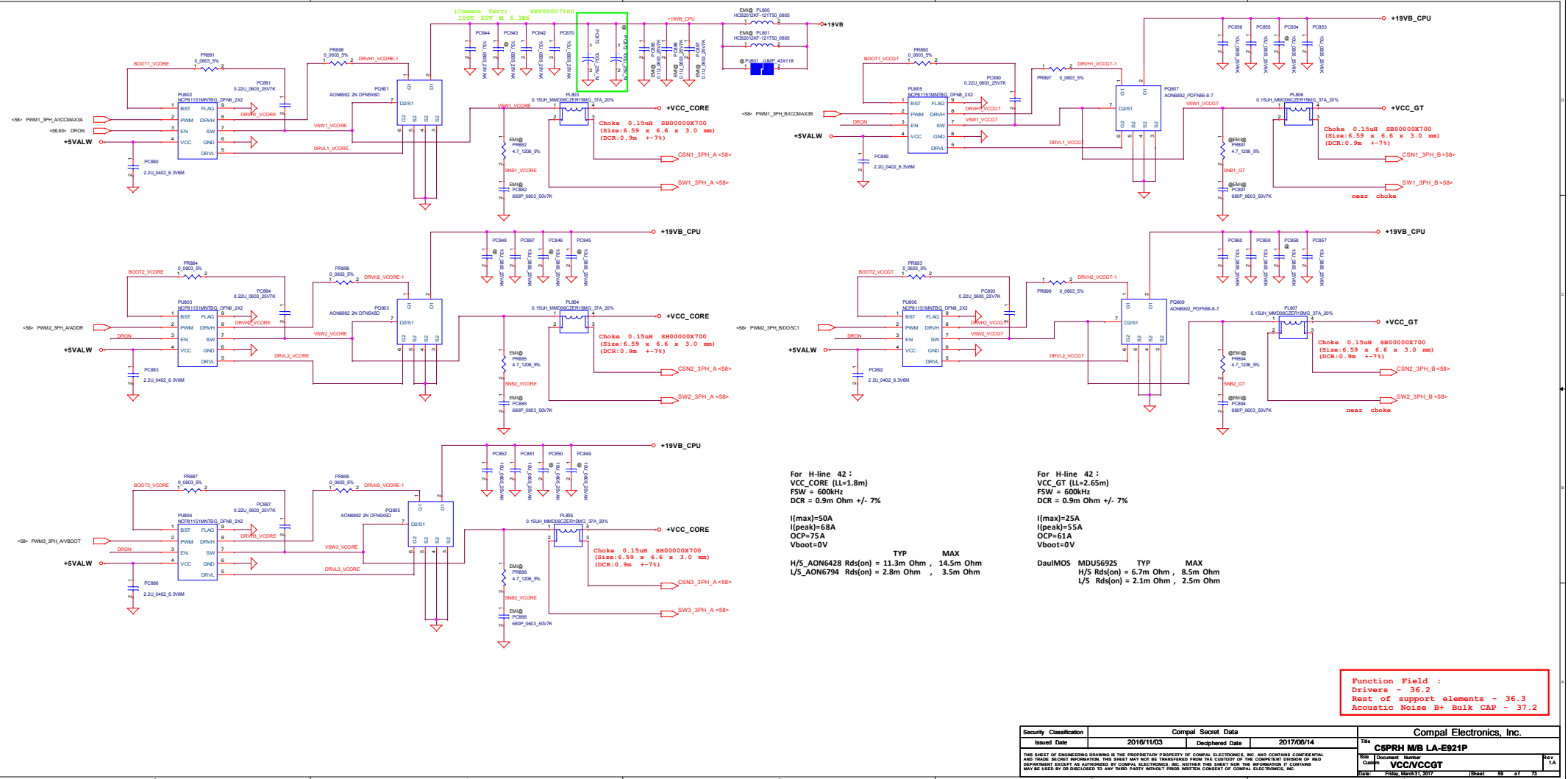


+1.5VSP:
Imax=0.5A Ipeak=0.75A

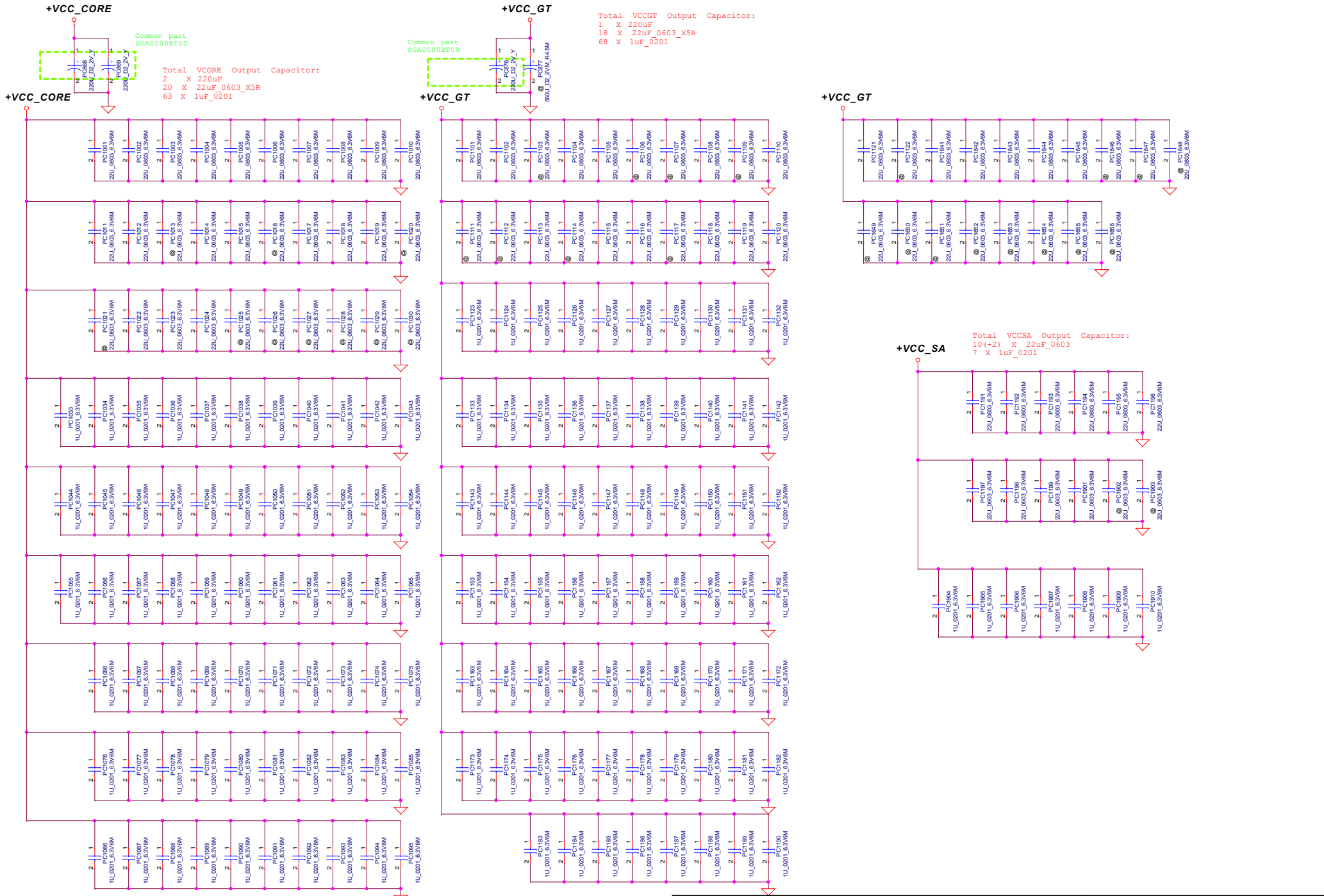
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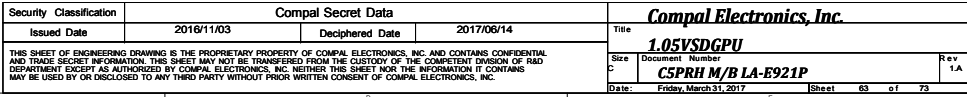


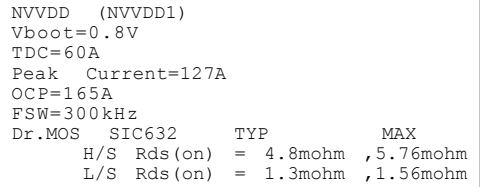
Total VCCGT Output Capacitor:
1 X 220uF
18 X 22uF 0603_X5R
68 X 1uF_0201

Total VCCGT Output Capacitor:
2 X 220uF
20 X 22uF 0603_X5R
63 X 1uF_0201

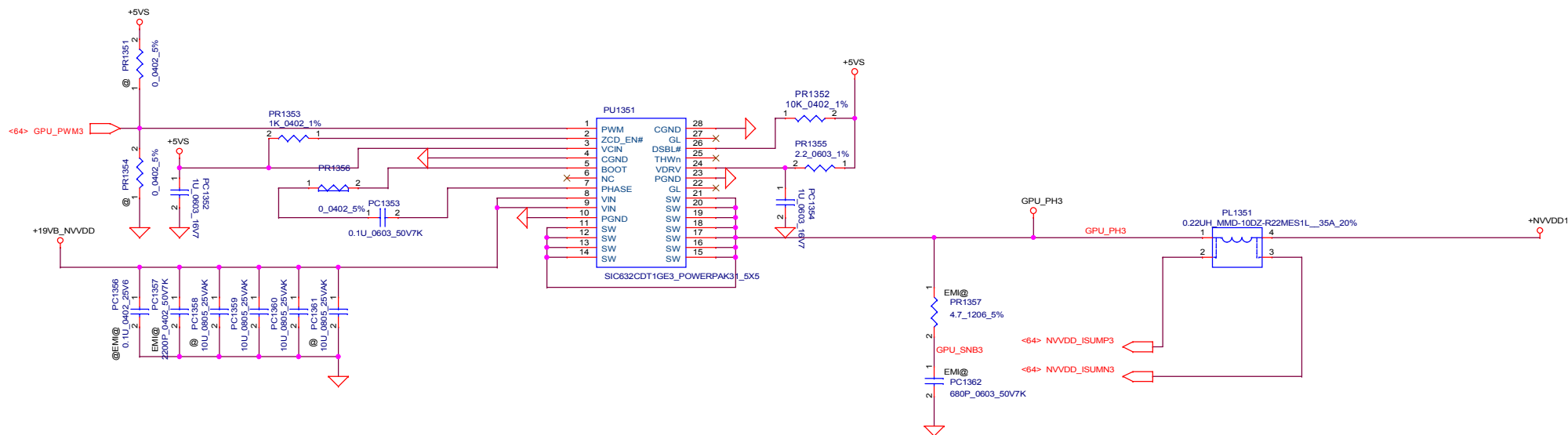
Total VCCSA Output Capacitor:
10(+2) X 22uF_0603
7 X 1uF_0201

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				Quantity	CPU CAP
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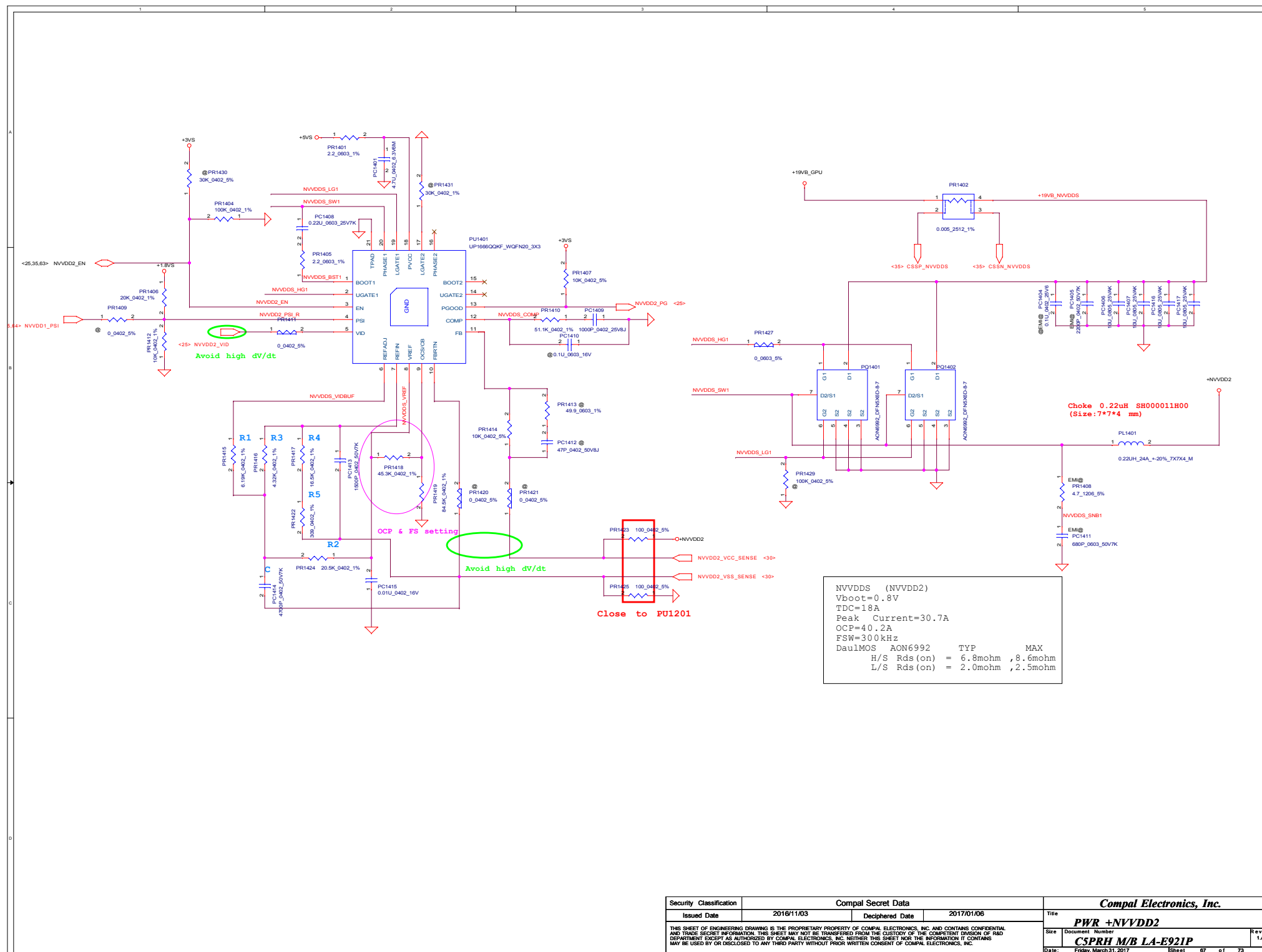


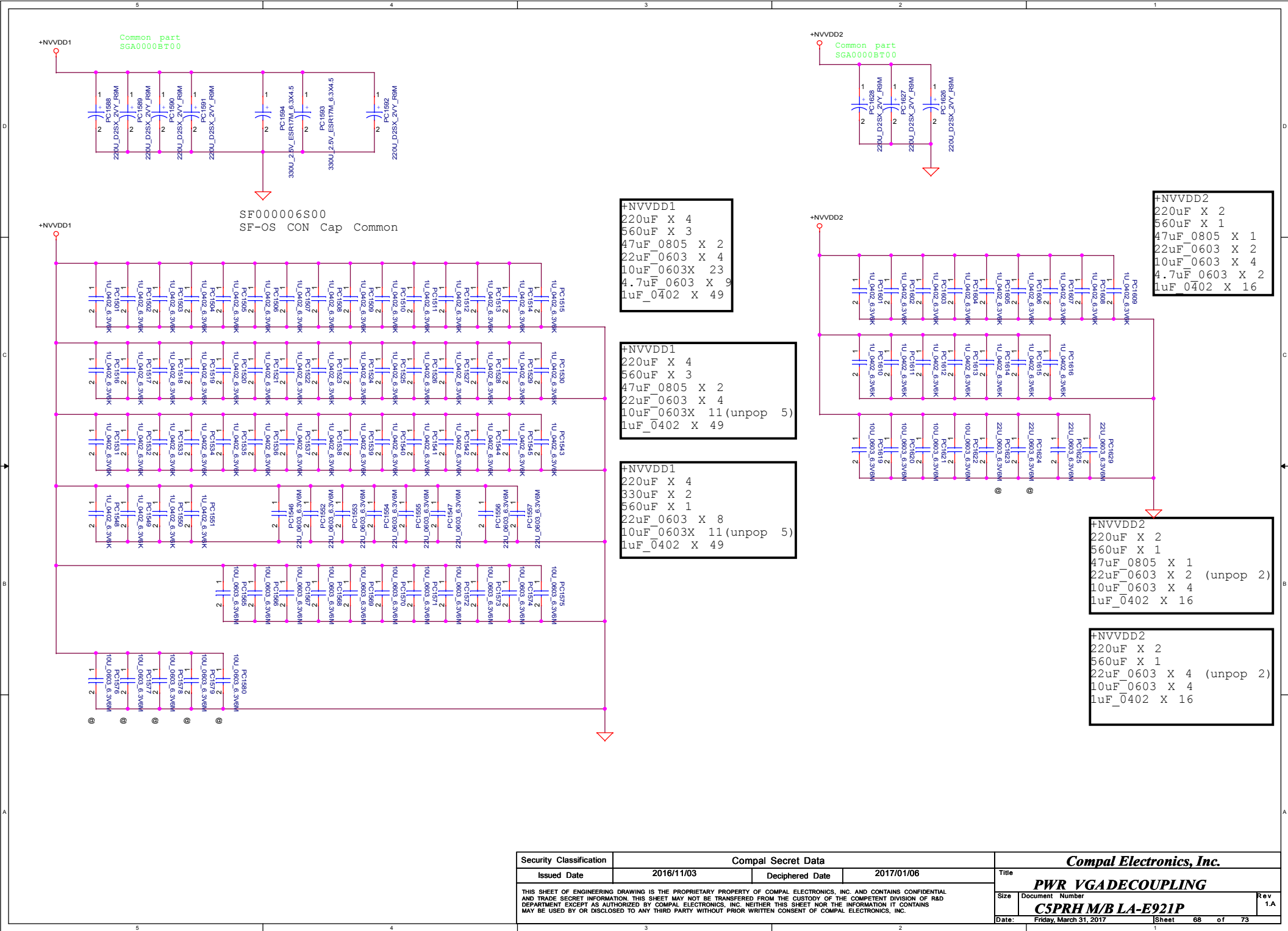
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								Size	Document Number			Rev 1A		
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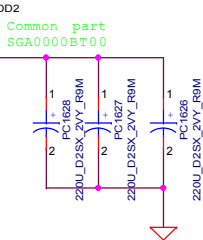


SF000006S00
SF-OS CON Cap Common

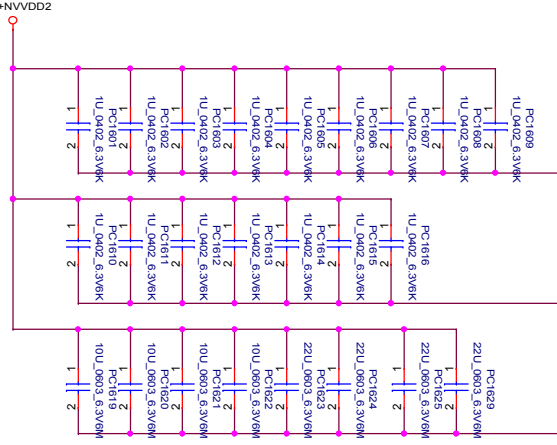
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220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 23
4.7uF_0603 X 9
1uF_0402 X 49

+NVVDD1
220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 11 (unpop 5)
1uF_0402 X 49

+NVVDD1
220uF X 4
330uF X 2
560uF X 1
22uF_0603 X 8
10uF_0603X 11 (unpop 5)
1uF_0402 X 49



+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2
10uF_0603 X 4
4.7uF_0603 X 2
1uF_0402 X 16



+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16

+NVVDD2
220uF X 2
560uF X 1
22uF_0603 X 4 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16

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				Document Number	1A
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